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On Highly Scalable 2-Level-Parallel Unstructured CFD

Jens Jägersküpper[1]

[1] German Aerospace Center DLR, 38108 Braunschweig, Germany
Institute of Aerodynamics and Flow Technology, https://dlr.de/as
Jens.Jaegerskuepper@DLR.de

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Exascale HPC systems are about to become available in near future. Such enormous simulation capabilities from the hardware perspective, however, require software that can effectively make efficient use of massively parallel hardware. For domain-decomposition based algorithms like CFD, it has become apparent that running one MPI process, i.e. one domain, per CPU core is no longer apt when there are hundreds of cores available per cluster node. There are too many processes per node that need to communicate with other remote processes. Message rates of network hardware simply have not kept up with the rate of increasing core count per node. Message aggregation is thus a key aspect of highly scalable parallel codes. A 2-level parallelization featuring a shared-memory level in addition to the MPI process level, resulting in significantly fewer communication connections between the nodes of an HPC cluster utilized by a simulation, seems a promising solution.

The CODA (CFD for ONERA, DLR, Airbus) software for high-fidelity compressible-flow simulations of industrial configurations implements such a 2-level domain-decomposition hybrid-parallel approach, which was adopted from the *Flexible Unstructured CFD Software (Flucs)* [1]. The processing of unstructured meshes is particularly challenging with respect to load balancing and non-linear data access. For maximum parallel scalability, CODA's parallelization not only features overlapping communication with computation on the process level, but also a dedicated Single Program (on) Multiple Data (SPMD) programming model on the shared-memory level, which make use of relaxed/local/partial synchronization of threads.

Here, the design principles of this parallelization concept are outlined, followed by details concerning the implementation of that concept in the *Flucs infrastructure (Flis)*, which has become part of CODA. Moreover, results of scalability studies with CODA are presented, which impressively demonstrate the extreme scalability realized with this parallelization approach. Finally, some aspects indicating potential for future improvements, which have been observed for the 1st-generation AMD EPYC$^{\text{TM}}$ architecture, are discussed.

REFERENCES

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