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RECONFIGURABLE SRTM SYSTEM FOR ROAD TRAFFIC IN KINGDOM OF BAHRAIN

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This paper presents reconfigurable hardware architecture for smart road traffic system based on Field Programmable Gate Array (FPGA). The design can be reconfigured for different timing of the traffic signals according to the received and collected data read by the different sensors on the road; the design has been described using VHDL (VHSIC Hardware Description Language). The SRTM (Smart Road Traffic Management) System has some more features that help passenger to avoid traffic jamming by sending the collected information through web/mobile applications to find the best road between the start and destination points, which will be displayed on Google maps, at the same time it will also shows the points of traffic jamming on Google maps. SRTM system can also manage emergency vehicles such as ambulance and fire fighter and also can send snapshots and video streaming for different roads and junctions to show the points of traffic jamming. The design has been simulated and tested using ModelSim PE student edition 10.4. Spartan 3 FPGA starter kit from Xilinx has been used for implementing and testing the design in a hardware level.

Keywords: FPGA; ITS; VHDL; Road Traffic

1. Introduction

Intelligent Transportation System (ITS) plays a key role in people's life, as their scope is to improve transportation safety and mobility and to enhance productivity through the use of advanced technologies (Anagnostopoulos *et al*., 2006). As the population and business activities are increased result in greater demand of vehicles for transportation, road traffic is getting more and more congested with limited resources of an existing infrastructures, the demands for a well developed ITS is also increased (Wiering e*t al*., 2004; Martinez *et al*., 2010). However city planning can help to avoid transportation problems, the unexpected growth in population and road usage makes city planning usually does not scale well over time (Martinez *et al.*, 2010; Song *et al*., 2012).

Traffic jamming is one of the main issues that people try to avoid in order to reduce the amount of wasted time, especially in the rush hours. Figure 1 shows Bahrain high way traffic jamming in the Rush hour. There are several studies and research projects related to intelligent transportation system and telematics that have been conducted globally to increase the flow of traffic and avoid traffic jamming as well as to increase the road safety, most of the related ITS projects have conducted in USA, Europe, Japan, China, and Korea, a few related ITS projects have been conducted in Arab countries (Giannopoulos and McDonald, 1997; Xu, 2000; Song *et al*., 2012; Ahonen and O'Reilly, 2007; Kolls, 2005; Hussain *et al.*, 2013; El-Medany and Hussain, 2007; Zaied and Al Othman, 2011).

In this paper a reconfigurable Smart Road Traffic Management System that organizes the Road Traffic in Kingdom of Bahrain is introduced. The objective of the research is to increase the traffic flow and find the best road for passengers in Kingdom of Bahrain and Gulf area in general, based on the existing infrastructure for most of the Gulf countries. The research also decreases the traffic congestion, especially in the rush hours; it also guides the passenger to search for the best road that gives a short time for his/her journey. It is not necessary to achieve a shortest time with the shortest route, as the developed system allocates the points of traffic jamming and post to a hosting server for visualization in an integrated Google maps in web/mobile applications.

The materials in this paper are organized as follows: in Section II, a discussion of related works is given; Section III, gives an overview of the system architecture; the hardware implementation is discussed in section IV; is given in Section V; in Section VI a discussion and simulation results is given; at the end, a conclusion will be given in Section VII.

Figure 1. Bahrain High Way traffic Jamming in the Rush hour

2. Related Works

Configurable technologies such as Field Programmable Gate Arrays (FPGAs) are widely used to accelerate design and prototyping. Moreover, with the dynamic reconfiguration property of the FPGAs, a low energy profile can be achieved in the designed system that realizes multiple applications in a time-multiplexed manner. Hence, a programmable heterogeneous Multi-Processor System-on-Chip (MPSoC) that contains an FPGA with multiple processing cores can be used to appropriately deal with the requirements of real-time computations (Karloff and Abdel-Raheem, 2013).

Reconfigurable hardware has many advantages and therefore it is used in many Intelligent Transportation Systems (ITS). FPGAs based Traffic light systems were developed and used as found in the literature (Zhenggang *et al*., 2009; El-Medany and Hussain, 2007). The researchers showed that FPGA based devices offer scalability, adaptability and stability and therefore can be a good solution for ITS systems. It also can increase the ITS efficiency (Zhenggang *et al.*, 2009). FPGAs was also used in implementing vehicle-to-vehicle communication (V2V) as in (Sander *et al*., 2009) who uses FPGA technology to implement a V2V communication system and uses special mechanisms that exploit its benefits.

Gorka Velez uses reconfigurable embedded vision system to implement a c lane departure warning system. The system contains a System on Chip composed of a programmable logic that supports parallel processing necessary for a fast pixel-level analysis. It also uses a microprocessor suited for serial decision making (Velez *et al*., 2014).

Other researchers such as Ricardo presented the design of a driver assistance system that provides Lane Detection, Lane-Change Detection and Obstacle Detection. The system is based on computer vision that provides information about the environment and the vehicle's current driving state. The core algorithms of the system have been realized as custom hardware co-processors to be executed on FPGA hardware, a soft-core CPU that performs general system control and final decision making based on co-processor output (Scarinci and Heydecker, 2014).

Javier Barrachina proposed the Density-based Road Side Unit (D-RSU) deployment policy which consists on placing RSUs according to an inverse proportion to the expected density to reduce the deployment cost (Barrachina *et al.*, 2012; Barrachina *et al*., 2013).

Sebastian presented a real-time video-based pedestrian detection system that uses multi-sensor architecture. The system can be used within a road side unit for intersection assistance. The system is implemented using available PC hardware, combining a frame grabber board with embedded FPGA and a graphics card into a powerful processing network (Bauer *et al*., 2010a). Sheldon presented a system that uses Virtex-5 Xilinx FPGA and hardware/software co-design tools to detect and recognizes traffic signs within a video stream (Han and Oruklu, 2014). Mihai presented a system with two units: the main controller unit, which was FPGA chip that and the Tag4M unit. The presented work by Mihai is to communicate with Traffic Servers in order to report traffic data or to receive commands (Hulea *et al*., 2011).

In all these FPGA based system a full capability smart traffic system is not implemented but in each system part of the traffic problems are tackled such as lane departure warning (Scarinci and Heydecker, 2014; Nieto *et al.*, 2014), driver assistance system, video-based pedestrian detection (Bauer *et al*., 2010b), traffic sign detection system (Waite and Oruklu, 2013). In the presented work an integrated smart transportation system with different capabilities using configurable hardware has been implemented. The objectives of the research are to design and implement an integrated smart transportation system that has the following capabilities: Real-time adaptive control traffic lights system; to maximize the flow of vehicles and reduce the waiting time while maintaining fairness among the other traffic lights; shows the points of traffic jamming on Google maps; manage emergency vehicles such as ambulance and fire fighter; Send snapshots and video streaming for different roads and junctions to show the points of traffic jamming.

3. Reconfigurable Architecture

Reconfigurable architecture becomes more attractive today as the target device for hardware implementation. The main advantage of reconfigurable architecture like Field Programmable Gate Arrays (FPGAs) is the ability of rapidly changing their hardware architecture to achieve different functionalities of their internal components and the interconnection between them to a customized design (Thanh *et al*., 2014). The main difference of reconfigurable architecture with the hardwired architecture like Application Specific Integrated Circuits (ASICs) is that the reconfigurable one can be modified and uploaded on the reconfigurable chip. However ASICs and FPGAs are both customized chips that are used for particular applications, the FPGAs as an example of reconfigurable architecture has an advantage of rapid prototyping compared to ASICs that takes more time for long fabrication processing steps; on the other hand FPGA does not require to reach the transistor level as ASICs design, however in FPGA the implemented design go through a process of generating a bit file (binary file) to be used for configuring the FPGA chip. PlanAhead is Xilinx software tools that are used for targeting FPGA implementation, Figure 2 shows PlanAhead Design Flows that produce the bit files as one its generated output.

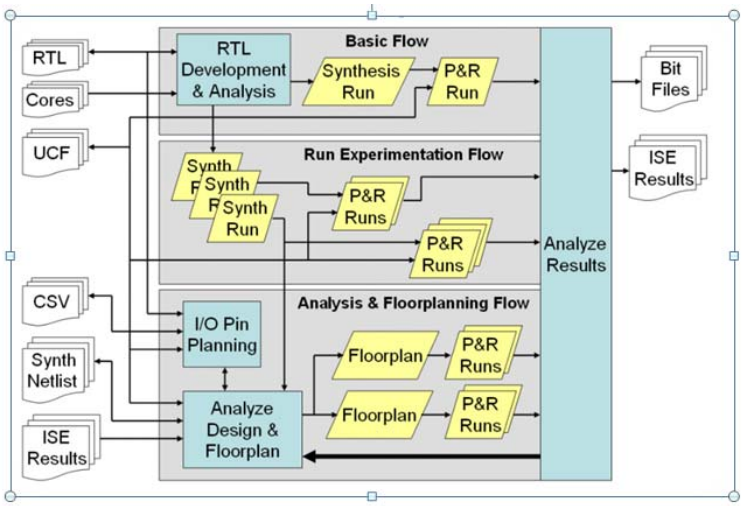


Figure 2. PlanAhead Design Flows (Xilinx, 2009)

4. SRTM System Architecture

The STRM System Architecture has three main components: the controller side, the web server and database side, and the traffic center and user side as shown in Figure 3. FPGA Main Controller, GPRS, Speed Camera, Traffic Signals, Red Light Camera, Traffic Sensors; Data Base, Web Server; Traffic Centre, User PC, User Laptop, User Mobil device. The main controller unit (FPGA) is interfaced to the traffic control part and the GPRS (General Packet Radio Service) as shown in Figure 4, the traffic control Process Flow is based on the state diagram of Figure 5. The state diagram in Figure 5 has 64 states that control the traffic flow based on timing and sensors at the same time, as well as display of remaining time for red or green signals, at the same time at has the action of red light crossing camera, speed camera, and also it send snap shots of the current state for the traffic, as well as sending life videos to the web server.

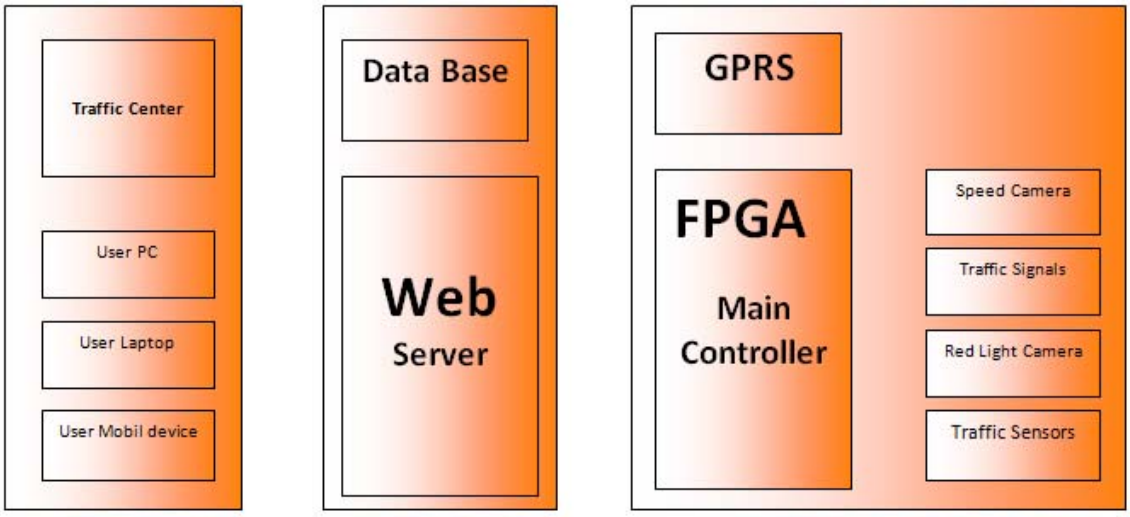


Figure 3. STRM System Architecture

Figure 4. The main controller unit Interface

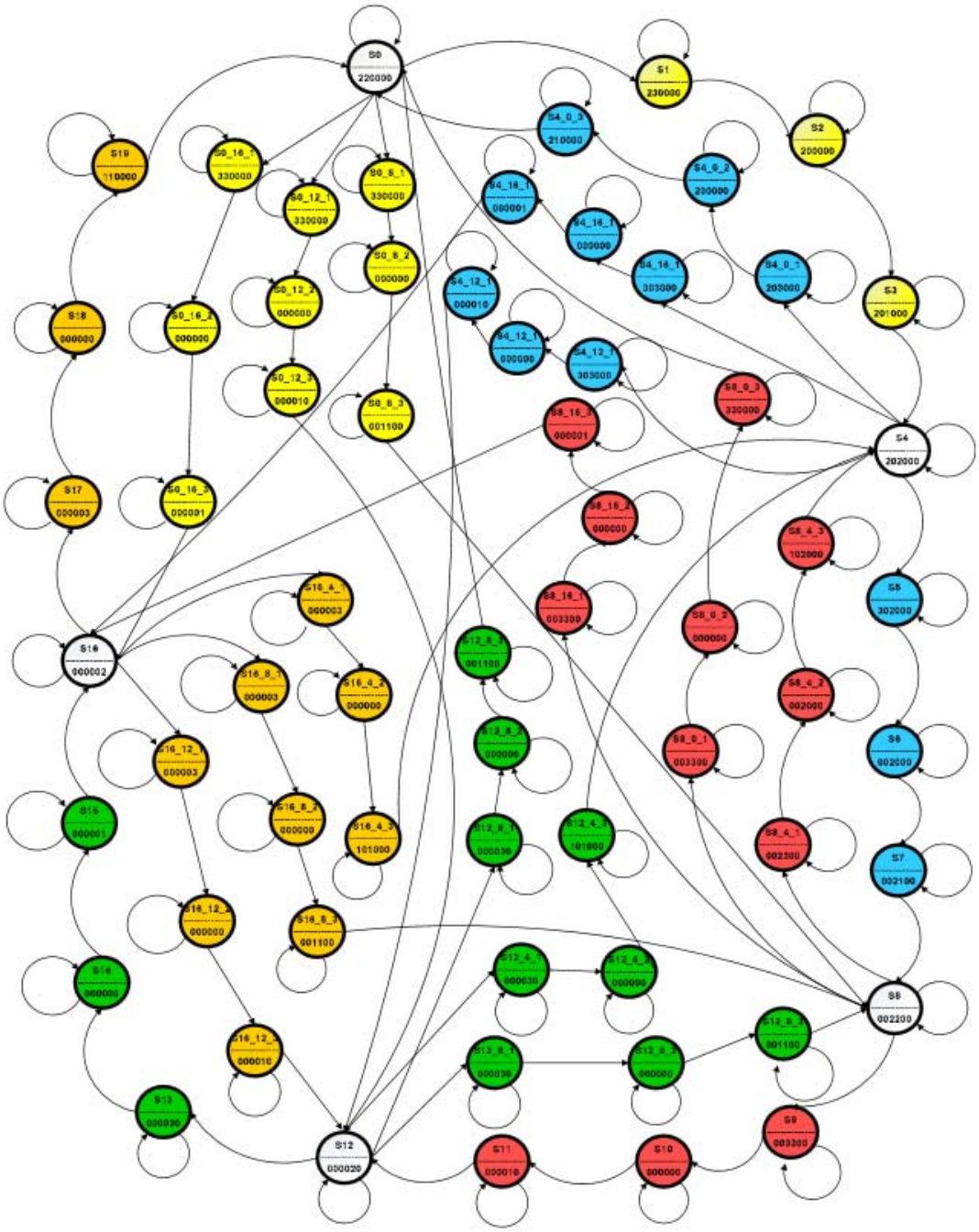


Figure 5. State Diagram for the Traffic Controll Process Flow (El-Medany and Hussain, 2007)

5. SRTM RTL System Design and Hardware Implementation

The hardware of SRTM has been designed using synthesizable VHDL code based on behavioural description. The VHDL description comprises the following functions: traffic signals control on timing bases, care detection, red light camera, speed camera, snapshot camera, video camera, and GPRS communications. The main controller is mainly an FPGA chip design interfaced to a group of sensors as inputs to the controller, and the outputs to different types of cameras and traffic signals, Fig. 6 shows a block diagram for the STRM hardware design.

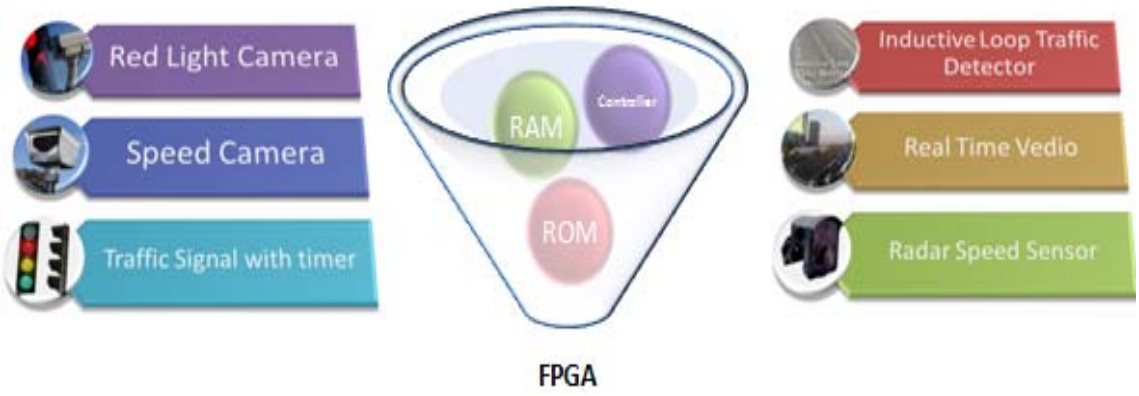


Figure 6. Block Diagram for the STRM Hardware Design

The synthesis process produces the Register Transfer Level (RTL), which is graphical representation of the HDL design module. The RTL produced by Xilinx Synthesis Technology (XST)) is generated by the synthesis tool. The goal of the RTL schematic view is to be as close as possible to the original VHDL code program. In the RTL schematic view, the design is represented in terms of basic building blocks, such as registers, multipliers, and adders. The VHDL code has been synthesized using XST (Xilinx Synthesis Technology) tools to produce netlist files (NGC files). The hardware implementation of the synthesized VHDL model for SRTM starts by the translate process, which merges the netlists and constraints into Xilinx NGD (Native Generic Database) design file, then mapping the design into the available resources on the target device such as CLBs and IOBs using the generated NGD file from the translate process to generate the NCD (Native Circuit Description) file that physically represents the design mapped to Xilinx FPGA target device, and then places and routes the design to the timing constraints, and finally creates a bitstream file (the bit file) that can be downloaded to the FPGA device. Figure 7, shows Xilinx VHDL synthesis process flow.

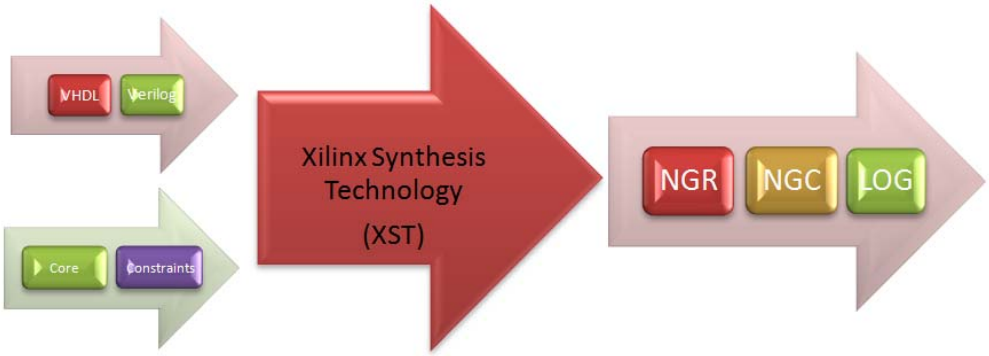


Figure 7. Xilinx Synthesis Process Flow

In order to perform specific function, the RTL design generates a set of control signals that will initiate a sequence of operations to perform the logic operation. Register transfer logic is a design abstraction that models the sequential circuits in terms of the flow of control signals between the generated memory registers. The registers synchronize the circuit's operation to the edges of the clock signal, and it is normally implemented as D flip-flops, and this is the memory part of the sequential circuit. There different types of Xilinx building block, most of them are Luck-Up Table (LUT). Figure 8 shows the generated RTL (Register Transfer Level) schematic of the SRTM system design, one of the main building block in Figure 8 is the LUTS_EAEE4044 that is shown in its gate level, in the top of Figure 8. Xilinx PlanAhead software tools offers a new improved user interface for RTL schematic that has a bit stream design flow with project management capabilities. Using PlanAhead, it is easy to improve design performance with floor planning. Figure (9-a) shows the annotated pins in SRTM system schematic view, however Figure (9-b) shows the SRTM logic hierarchy in schematic view (Abdallah *et al*., 2015; Sharma *et al*., 2015).

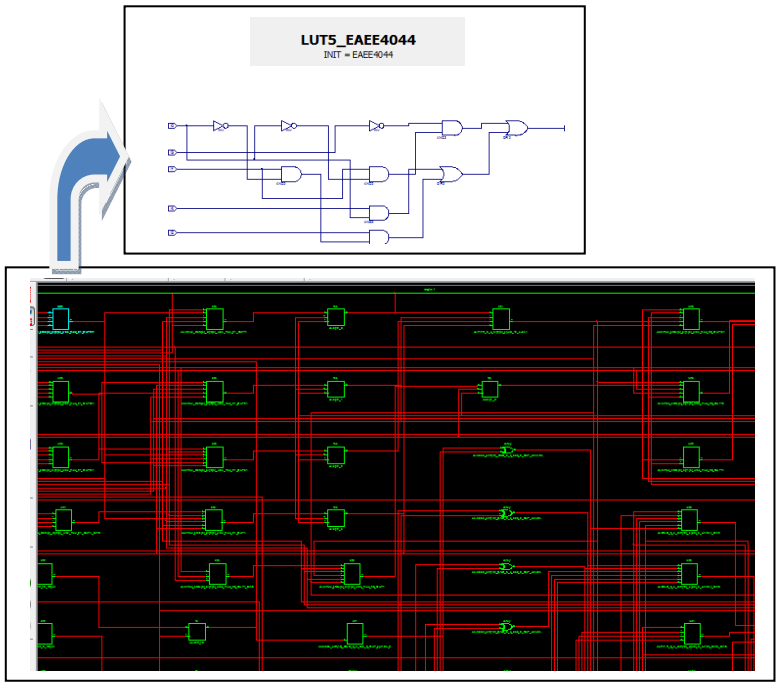
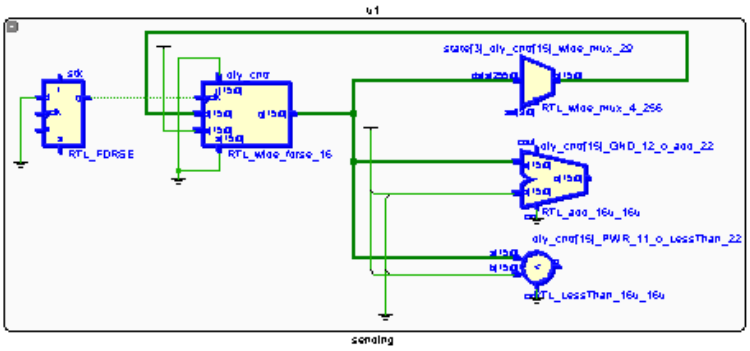
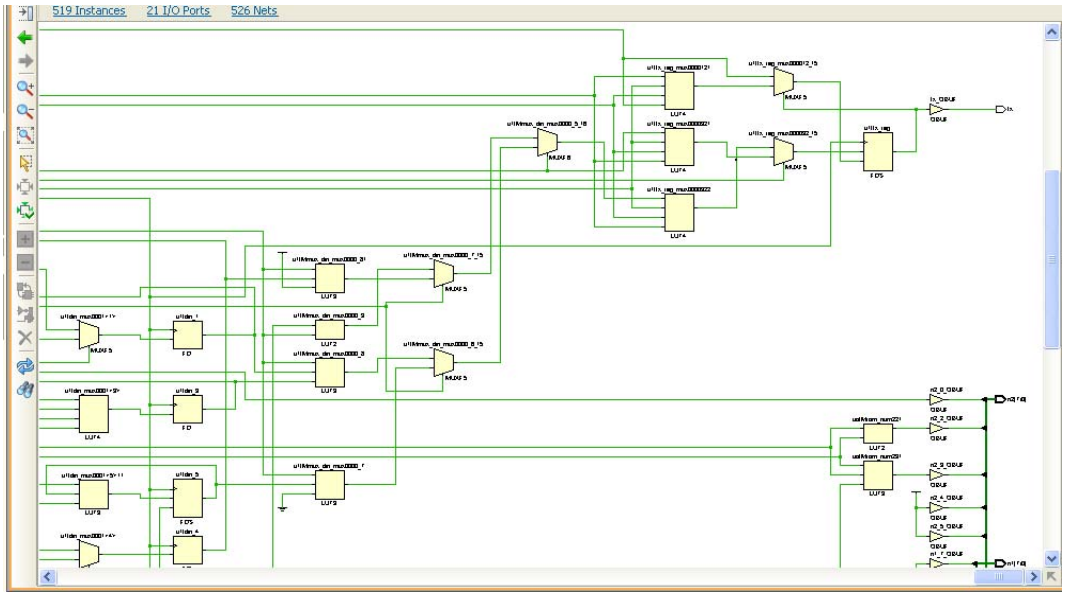


Figure 8. RTL Schematic for SRTM System Design



a. Annotated Pins



b. Schematic Logic Hierarchy SRTM

Figure 9. SRTM System Schematic View

6. Conclusions

In this paper reconfigurable hardware architecture for Smart Road Traffic System is presented. The system is based on Field Programmable Gate Array (FPGA) and has been described using VHDL (VHSIC Hardware Description Language). The proposed architecture has many advantages such as the design can be reconfigured for different timing of the traffic signals according to the received and collected data from the road. The SRTM System has some more features that help passenger to avoid traffic jamming by sending the collected information through web/mobile applications to find the best road between the start and destination points, which will be displayed on Google maps, at the same time it will also shows the points of traffic jamming on Google maps. SRTM system can also manage emergency vehicles such as ambulance and fire fighter and also can send snapshots and video streaming for different roads and junctions to show the points of traffic jamming. The design has been simulated and tested using ModelSim PE student edition 10.4. Spartan 3 FPGA starter kit from Xilinx has been used for implementing and testing the design in a hardware level. The system was implemented and tested on Kingdom of Bahrain and proved to be effective and affordable.

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