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A New Three-Level Flying-Capacitor Boost Converter with an Integrated LC^2D Output Network for Fuel-Cell Vehicles: Analysis and Design

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Abstract: In this paper, a new three-level boost converter with continuous input current, common ground, reduced voltage stress on the power switches, and wide voltage gain range is proposed. The proposed converter is composed of a three-level flying-capacitor switching cell and an integrated LC^2D output network. The LC^2D output network enhances the voltage gain of the converter and reduces the voltage stress on the power switches. The proposed converter is a good candidate to interface fuel cells to the dc-link bus of the three-phase inverter of an electric vehicle (EV). A full steady-state analysis of the proposed converter in the continuous conduction mode (CCM) is given in this paper. A 1.2 kW scaled-down laboratory setup was built using gallium nitride (GaN) transistors and silicon carbide (SiC) diodes to verify the feasibility of the proposed converter.

Keywords: boost converter; multilevel; wide-bandgap; GaN; SiC; canonical switching cell; flying capacitor; renewable energy; fuel cells; electric vehicles

1. Introduction

There is a growing global interest in reducing greenhouse gases by developing new clean energy technologies that address the challenges associated with the increasing penetration of renewable energy systems and the need to reduce fossil fuel consumption. The increasing number of automobiles worldwide is a growing problem, because they contribute to air pollution. A lot of research and development is being targeted to develop new fully electric vehicles (EVs) powered by clean energies. Fuel cell-powered EVs are a big contributor to the electrification of automobiles. Fuel cells, as a source of electrical energy, have the following features: pollution-free operation, high-density current output, and high efficiency [1]. The fuel cell has a low output voltage, which requires a step-up dc–dc converter with a high-voltage gain to solve the voltage mismatch between the fuel cell and the dc-link bus of the three-phase inverter inside a car [2–9]. Fuel cells are unlike batteries, as they have soft output characteristics, in that their output voltage drops drastically when the output current increases [2]. The architecture of a fuel cell-powered EV with a step-up converter is shown in Figure 1. This converter steps up the voltage of the fuel cell to the level required by the three-phase inverter, and the inverter drives the electric motor. The step-up converter should have the following features: wide voltage gain range, high efficiency, small size, low weight, and low input current ripple [10].

The conventional boost converter, theoretically, has an infinite voltage gain at unity duty cycle; however, due to the parasitic resistance in the passive component, the maximum gain is much lower, and the maximum gain keeps decreasing as the load current increases [11,12].

Many of the topologies of high-gain step-up dc–dc converters have been introduced in the literature [9,13–20]. Some of these topologies rely on switched capacitor networks [16,17,21]

and voltage lift networks [18,19] to extend the voltage gain. The main disadvantage of these topologies is the high current flowing through the semiconductor devices due to the capacitor networks, which result in reduced efficiency.

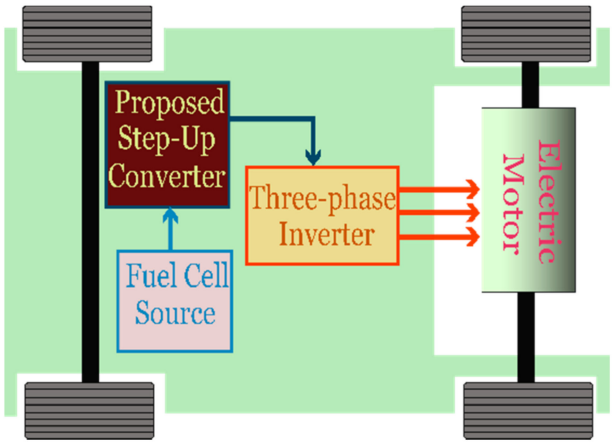

Figure 1. A fuel cell-powered electric vehicle (EV) with the proposed converter.

Other topologies rely on magnetic coupling to obtain a high-voltage gain [10,14,22,23]. The main drawback of these topologies is the high voltage spikes across the main switches because of the leakage inductance of the magnetic coupling component. Also, the size of the magnetic coupling component decreases the power density and the specific power of the step-up dc–dc converter.

Multilevel architectures have gained a lot of interest, especially, in the past decade, as they distribute the voltage stress across semiconductor devices, which enables the utilization of semiconductor devices with low-rated voltage; thus, the efficiency can be enhanced.

The conventional three-level boost (TLB) was discussed in [20]. This TLB converter reduces the voltage stress across the semiconductor devices to half the output voltage, which enables the utilization of low-voltage transistors with low on-resistance (R_{on}), resulting in higher efficiency and lower cooling system requirement. Also, this TLB converter has an input current with double the switching frequency; hence, a smaller input inductor can be used. The conventional TLB converter has two major drawbacks:

(1) It has the same voltage gain of the conventional boost converter, which means it has a limited maximum voltage gain; and
(2) It requires an external voltage balancing controller (to balance out the voltages across the power switches), which increases the system complexity.

The flying-capacitor switching network is the most commonly adopted multilevel architecture due to its simple circuit structure and inherent voltage balance without the need for extra circuitries.

In this paper, a new non-isolated three-level flying-capacitor boost converter with an integrated LC^2D output network is proposed. This proposed converter has a higher voltage gain and puts less voltage stress on the power switches compared with the conventional three-level flying-capacitor boost converter. An experimental prototype was built and tested to verify the performance of the proposed converter.

This paper is divided into six sections and organized as follows: Section 2 discusses the structure and the operating principles of the proposed converter, Section 3 presents the components' parameters design, Section 4 shows the loss analysis of the various components, Section 5 presents the experimental results, and finally, the conclusion is presented in Section 6.

2. Structure and Operating Principles of the Proposed Converter

2.1. General Structure of the Proposed Converter

The proposed converter is presented in Figure 2, where it is composed of two active switches (Q_1, Q_2), three diodes (D_1, D_2, D_3), two inductors (L_1, L_2), and four capacitors (C_1, C_2, C_3, C_4). The fuel cell is depicted as a dc voltage source (V_{in}). The network of (Q_1, Q_2, D_1, D_2, C_2, C_3) forms a three-level flying-capacitor switching cell. The LC^2D output network enhances the voltage gain and reduces the voltage stress on the power switches.

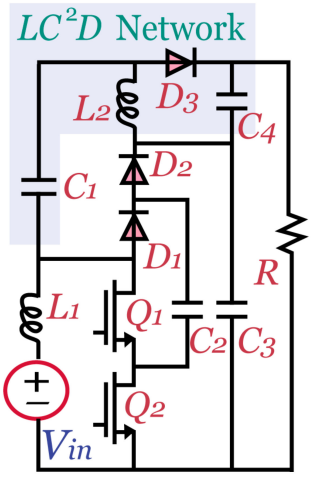

Figure 2. The schematic of the proposed converter.

2.2. Operation Modes

The proposed converter has two active switches; hence, it has four possible switching states for Q_1 and Q_2. These switching states are S_1S_2 = {00, 01, 10, and 11}, as S_1 and S_2 are the triggering signals of Q_1 and Q_2, respectively.

The triggering signals S_1 and S_2 are generated via comparing two phase-shifted 180° carrier signals with a modulation signal (D). This means that there are three possible switching sequences based on the value of D. When $D > 0.5$, the switching sequence of S_1S_2 is {10, 11, 01, 11, and 10}. When $D < 0.5$, the switching sequence of S_1S_2 is {10, 00, 01, 00, and 10}. When $D = 0.5$, the switching sequence of S_1S_2 is {10, 01, and 10}. The current flow paths when $D < 0.5$ and $D > 0.5$ are shown in Figures 3 and 4, respectively, and the key waveforms of the proposed TLB converter are presented in Figure 5.

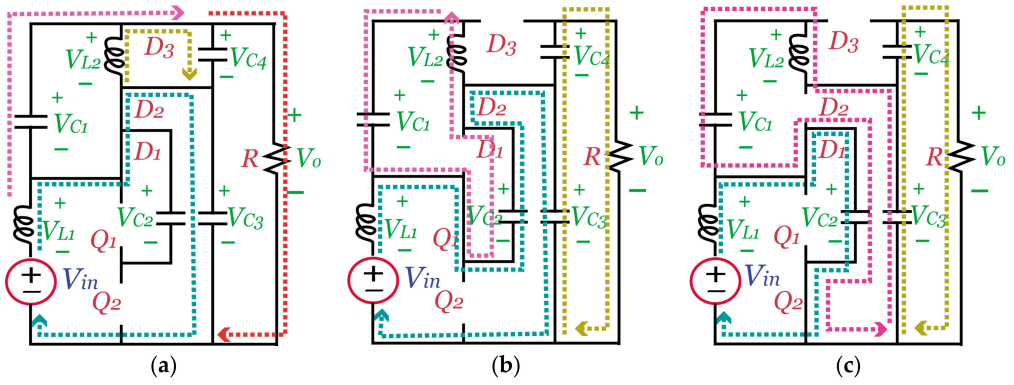

Figure 3. Current flow paths when $D < 0.5$. (**a**) S_1S_2 = 00. (**b**) S_1S_2 = 10. (**c**) S_1S_2 = 01.

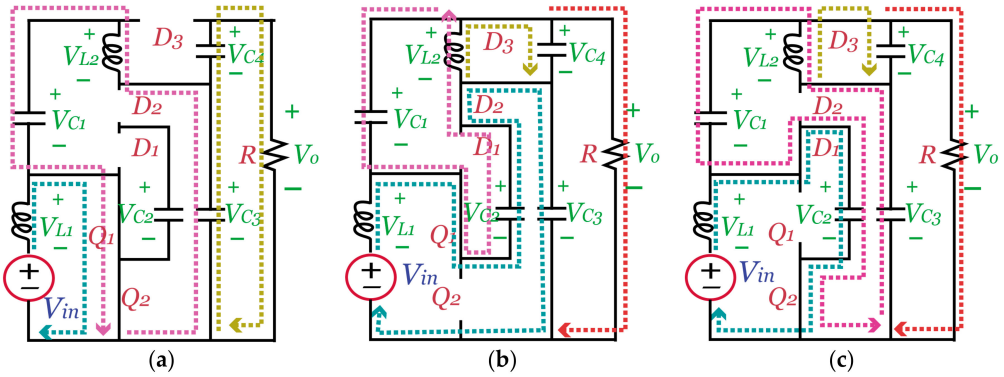

Figure 4. Current flow paths when $D > 0.5$. (**a**) $S_1S_2 = 11$. (**b**) $S_1S_2 = 10$. (**c**) $S_1S_2 = 01$.

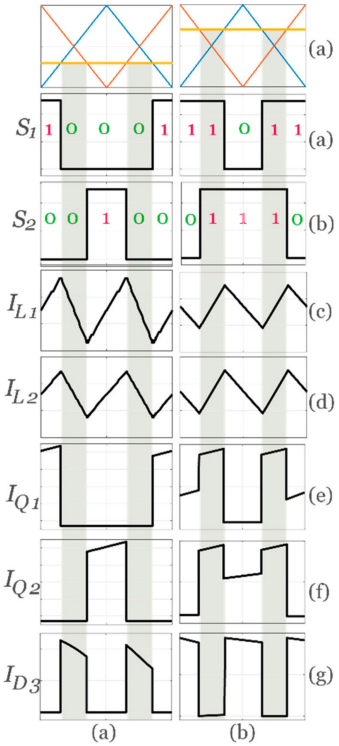

Figure 5. Key waveforms of the proposed converter (**a**) $D < 0.5$. (**b**) $D > 0.5$.

2.3. Analysis of the Switching States

In this subsection, the proposed converter is analyzed during each of the four switching states to be used after that in calculating the voltage gain and the voltage stress associated with each switching sequence.

When $S_1S_2 = 01$, as shown in Figures 3c and 4c, by applying the Kirchhoff's voltage law (KVL), we obtain Equations (1) and (2).

$$V_{L1} = V_{in} - V_{c2} \tag{1}$$

$$V_{L2} = V_{C1} + V_{C2} - V_{C3} \tag{2}$$

When $S_1S_2 = 10$, as shown in Figures 3b and 4b, by applying the KVL, we obtain Equations (3) and (4).

$$V_{L1} = V_{in} + V_{C2} - V_{C3} \tag{3}$$

$$V_{L2} = V_{C1} - V_{C2} \tag{4}$$

When S_1S_2 = 11, as shown in Figure 4a, by applying the KVL, we obtain Equations (5) and (6).

$$V_{L1} = V_{in} \tag{5}$$

$$V_{L2} = V_{C1} - V_{C3} \tag{6}$$

When S_1S_2 = 00, as shown in Figure 3a, by applying the KVL, we obtain Equations (7) and (8).

$$V_{L1} = V_{IN} - V_{C3} \tag{7}$$

$$V_{L2} = V_{C1} \tag{8}$$

2.4. Wide Voltage Gain

In this subsection, the voltage gain of the proposed converter is derived for $D > 0.5$ and $D < 0.5$. To simplify the analysis, all the inductors and capacitors are assumed to be ideal and very large to apply the small ripple approximation. When $D > 0.5$, as shown in Figure 6b, the switching sequence of S_1S_2 is {10, 11, 01, 11, and 10}. In this switching sequence the time of state {01}, T_{01}, the time of state {10}, T_{10}, and the time of state {11}, T_{11}, are defined as shown in Equation (9):

$$\begin{cases} T_{01} = (1-D)T \\ T_{10} = (1-D)T \\ T_{11} = (2D-1)T \end{cases} \tag{9}$$

As T is the periodic time of the carrier signals.

By applying the volt-second balance rule on L_1 and L_2, we obtain Equations (10) and (11):

$$V_{C3} = \frac{V_{in}}{1-D} \tag{10}$$

$$V_{C1} = \frac{D}{1-D} \cdot V_{in} \tag{11}$$

The output voltage V_o can be defined as the biggest value of the sum of "V_{C3}" and "V_{L2}". Thus, when $D > 0.5$, V_o can be calculated as the following:

$$V_o = V_{C3} + V_{C1} - V_{C2} \tag{12}$$

Because C_2 and C_3 are the two capacitors of a three-level flying capacitor network, V_{C2} is half V_{C3}; hence, the following is true:

$$V_0 = \frac{V_{C3}}{2} + V_{c1} \tag{13}$$

By substituting by Equations (10) and (11) in Equation (13), we obtain the following:

$$V_0 = \frac{0.5 + D}{1-D} V_{in} \tag{14}$$

Thus, the voltage gain, M, is defined by Equation (15) as follows:

$$M = \frac{V_o}{V_{in}} = \frac{0.5 + D}{1-D} \tag{15}$$

When $D < 0.5$, as shown in Figure 6a, the switching sequence of S_1S_2 is {10, 00, 01, 00, and 10}. In this switching sequence T_{01}, T_{10}, and the time of state {00}, T_{00}, are defined as follows:

$$\begin{cases} T_{01} = DT \\ T_{10} = DT \\ T_{00} = (1-2D)T \end{cases} \tag{16}$$

By applying the volt-second balance rule on L_1 and L_2, we obtains Equations (17) and (18):

$$V_{C3} = \frac{V_{in}}{1-D} \tag{17}$$

$$V_{C3} = \frac{D}{1-D} \cdot V_{in} \tag{18}$$

In this switching sequence V_o can be defined as the biggest value of the sum of "V_{C3}" and "$-V_{L2}$". Thus, when $D < 0.5$, V_o can be calculated as the following:

$$V_o = V_{C3} + V_{C1} \tag{19}$$

By substituting by Equations (17) and (18) in Equation (19), we obtain the following:

$$V_0 = \frac{1+D}{1-D} \cdot V_{in} \tag{20}$$

Thus, the voltage gain, M, is defined by Equation (21):

$$M = \frac{V_o}{V_{in}} = \frac{1+D}{1-D} \tag{21}$$

The equations derived for the $D > 0.5$ case can be applied for $D = 0.5$.

When S_1S_2 is {10, or 01}, the states of L_1 and L_2 depend on the value of D. From Equations (1)–(4), the voltage across L_1 and L_2 can be defined as the following:

$$V_{L1} = \frac{0.5-D}{1-D} \cdot V_{in} \tag{22}$$

$$V_{L2} = \frac{D-0.5}{1-D} \cdot V_{in} \tag{23}$$

By means of Equations (22) and (23) and the voltage polarities shown in Figures 3 and 4, both L_1 and L_2 are charging when D is less than 0.5, while they are discharging when D is greater than 0.5.

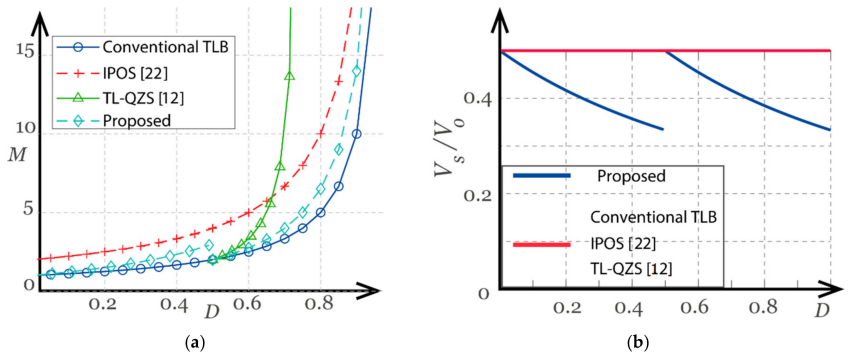

Figure 6. Comparison between the proposed converter and other step-up converters. (**a**) Gain vs. duty cycle. (**b**) Voltage stress vs. duty cycle.

2.5. Voltage Stress Analysis

2.5.1. Voltage Stress across the Capacitors

The voltages across C_4 equals ($V_o - V_{C3}$). The voltages across C_1, C_2, and C_3 are described by Equations (24) and (25) as follows:

$$V_{C2} = \frac{V_{C3}}{2} = \begin{cases} \frac{V_o}{2(1+D)} & D < 0.5 \\ \frac{V_o}{1+2D} & D \geq 0.5 \end{cases} \tag{24}$$

$$V_{C1} = \begin{cases} \frac{D\ V_o}{(1+D)} & D < 0.5 \\ \frac{D\ V_o}{(0.5+D)} & D \geq 0.5 \end{cases} \tag{25}$$

2.5.2. Voltage Stress across the Semiconductor Devices

The voltage across Q_1, Q_2, D_1, D_2, and D_3 can be expressed by Equation (26).

$$V_{Q1} = V_{Q2} = V_{D1} = V_{D2} = V_{D3} = \frac{V_{C3}}{2} = \begin{cases} \frac{V_o}{2(1+D)} & D < 0.5 \\ \frac{V_o}{1+2D} & D \geq 0.5 \end{cases} \tag{26}$$

2.6. Current Stress Analysis

In this subsection the current stresses on both the semiconductor devices and inductors are derived. The analysis is divided into two parts, depending on the value of D. In the following equations, the output load current is I_o, the average currents of inductors L_1 and L_2 are I_{L1} and I_{L2}, respectively, the average charging currents of capacitors C_1, C_2, C_3, and C_4 are I_{C1_ch}, I_{C2_ch}, I_{C3_ch}, and I_{C4_ch}, respectively, and the average discharging currents of capacitors C_1, C_2, C_3, and C_4 are I_{C1_disch}, I_{C2_disch}, I_{C3_disch}, and I_{C4_disch}, respectively.

2.6.1. For $D > 0.5$

The current stresses can be obtained as follows.

In the $S_1S_2 = 11$ switching state, C_3 discharges, C_1 charges, C_2 neither charges nor discharges, and C_4 discharges. Diode D_3 is reverse biased. By applying Kirchhoff's current law (KCL), the relationships between the inductor and capacitor currents can be expressed as follows:

$$I_{C3\_disch} = -I_{L2} \tag{27}$$

$$I_{C1\_ch} = -I_{L2} \tag{28}$$

$$I_{C4\_disch} = -I_{L2} = -I_o \tag{29}$$

In the $S_1S_2 = 10$ switching state, C_3 charges, C_1 discharges, C_2 discharges, and C_4 charges. Diode D_3 is forward biased. Thus, we obtain the following equations:

$$I_{C3\_ch} = -I_{C2\_disch} - I_{L2} \tag{30}$$

$$I_{C4\_ch} = I_{C1\_disch} \tag{31}$$

$$I_{C1\_disch} = -I_{C2\_disch} + I_{L1} \tag{32}$$

In the $S_1S_2 = 01$ switching state, C_3 discharges, C_1 discharges, C_2 charges, and C_4 charges. Diode D_3 is forward biased. We obtain the following equations:

$$I_{C3\_disch} = -I_{L2} \tag{33}$$

$$I_{C4\_ch} = I_{C1\_disch} \tag{34}$$

$$I_{C1\_disch} = -I_{C2\_ch} + I_{L1} \tag{35}$$

By using the capacitor charge-second balance rule on capacitors C_1, C_2, C_3, and C_4, the following relationships can be obtained:

$$I_{C1\_disch} = \frac{2D-1}{2(1-D)} \cdot I_{L2} \tag{36}$$

$$I_{C2\_ch} = -I_{C2\_disch} = I_{L1} - I_{C1\_disch} \tag{37}$$

$$I_{C3\_ch} = -I_{C2\_disch} - I_{L2} \tag{38}$$

$$I_{C4\_ch} = I_{L2} + I_{C1\_disch} - I_o \tag{39}$$

$$I_{L2} = I_o \tag{40}$$

Assuming a lossless operation, the relationship between I_o and I_{L1} can be obtained as follows:

$$V_{in}\ I_{L1} = V_o\, I_o \tag{41}$$

$$I_{L1} = \frac{(0.5+D)Io}{(1-D)} \tag{42}$$

When $D > 0.5$, diode D_3 conducts only during S_1S_2 = {10, and 10}, and the instantaneous current flowing through D_3 during T_{01} and T_{10} is I_{D3}. During S_1S_2 = {11}, the instantaneous current flowing through Q_1 and Q_2 is I_{Q_11}. During S_1S_2 = {10}, the instantaneous currents flowing through Q_1, Q_2, D_1, and D_2 are I_{Q1_10}, I_{Q2_10}, I_{D1_10}, and I_{D2_10}, respectively. During S_1S_2 = {01}, the instantaneous currents flowing through Q_1, Q_2, D_1, and D_2 are I_{Q1_01}, I_{Q2_01}, I_{D1_01}, and I_{D2_01}, respectively.

$$I_{D3} = \frac{1}{2(1-D)} \cdot I_{L2} \tag{43}$$

$$I_{Q\_11} = I_{L1} + I_{L2} \tag{44}$$

$$I_{Q1\_10} = I_{Q2\_01} = I_{D2\_10} = I_{D1\_01} = I_{C2\_ch} \tag{45}$$

$$I_{Q1\_01} = I_{Q2\_10} = I_{D1\_10} = I_{D2\_01} = 0 \tag{46}$$

The root-mean-square (rms) values of currents flowing through the components of the converter are essential for loss analysis. The rms values of I_{Q1}, I_{Q2}, I_{D1}, I_{D2}, I_{D3}, I_{C1}, I_{C2}, I_{C3}, and I_{C4} are I_{Q1_rms}, I_{Q2_rms}, I_{D1_rms}, I_{D2_rms}, I_{D3_rms}, I_{C1_rms}, I_{C2_rms}, I_{C3_rms}, and I_{C4_rms}, respectively. Using Equations (9), (27)–(46) we can obtain the following equations:

$$I_{Q1\_rms} = I_{Q2\_rms} = \sqrt{(2D-1)(I_{L1}+I_{L2})^2 + (1-D)(I_{L1}-I_{C1\_disch})^2} \tag{47}$$

$$I_{D1\_rms} = I_{D2\_rms} = \sqrt{(1-D)(I_{L1}-I_{C1\_disch})^2} \tag{48}$$

$$I_{D3\_rms} = I_{L2} = I_o \tag{49}$$

$$I_{C1\_rms} = \sqrt{(2D-1)(I_{L2})^2 + 2(1-D)\left(\frac{2D-1}{2(1-D)} I_{L2}\right)^2} \tag{50}$$

$$I_{C2\_rms} = \sqrt{2(1-D\ )(I_{L1}-I_{C1\_disch})^2} \tag{51}$$

$$I_{C3\_rms} = \sqrt{(D)(I_{L2})^2 + (1-D)(I_{C2\_disch}-I_{L2})^2} \tag{52}$$

$$I_{C4\_rms} = \sqrt{(2D-1)(I_o)^2 + 2(1-D)(I_{C1\_disch})^2} \tag{53}$$

2.6.2. For $D < 0.5$

The current stresses can be obtained as follows.

In the $S_1S_2 = 00$ switching state, C_3 charges, C_1 discharges, C_2 neither charges nor discharges, and C_4 charges. Diode D_3 is forward biased. By applying the KCL rule, the relationships between the inductor and capacitor currents can be expressed as follows:

$$I_{C3\_ch} = I_{L1} - I_{C1\_disch} - I_{L2} \tag{54}$$

$$I_{C4\_ch} = I_{L2} + I_{C1\_disch} - I_o \tag{55}$$

In the $S_1S_2 = 10$ switching state, C_3 charges, C_1 charges, C_2 discharges, and C_4 discharges. Diode D_3 is reverse biased. We obtain the following equations:

$$I_{C3\_ch} = -I_{C2\_disch} - I_{L2} = I_{L1} \tag{56}$$

$$I_{C2\_disch} = -I_{L1} - I_{L2} \tag{57}$$

$$I_{C1\_ch} = -I_{L2} \tag{58}$$

In the $S_1S_2 = 01$ switching state, C_3 discharges, C_1 charges, C_2 charges, and C_4 discharges. Diode D_3 is reverse biased. We obtain the following equations:

$$I_{C3\_disch} = -I_{L2} \tag{59}$$

$$I_{C2\_ch} = I_{L1} + I_{L2} \tag{60}$$

$$I_{C1\_ch} = -I_{L2} \tag{61}$$

By using the capacitor charge-second balance rule on capacitors C_1, C_2, C_3, and C_4, the following relationships can be obtained:

$$I_{C1\_disch} = \frac{2D}{1-2D} \cdot I_{L2} \tag{62}$$

$$I_{C2\_ch} = -I_{C2\_disch} = I_{L1} + I_{L2} \tag{63}$$

Assuming a lossless operation and using Equation (41), the relationship between I_o and I_{L1} can be obtained by the following:

$$I_{L1} = \frac{(1+D)Io}{(1-D)} \tag{64}$$

When $D < 0.5$, diode D_3 conducts only during $S_1S_2 = \{00\}$, and the instantaneous current flowing through D_3 during T_{00} is I_{D3_00}. During $S_1S_2 = \{00\}$, the instantaneous current flowing through D_3 is I_{D3_00}. The relationship between the transistor, diode, and inductor currents can be obtained by the following:

$$I_{D3\_00} = \frac{1}{1-2D} \cdot L_{L2} \tag{65}$$

$$I_{Q1\_10} = I_{Q2\_01} = I_{D2\_10} = I_{D1\_01} = I_{L1} + I_{L2} \tag{66}$$

$$I_{Q1\_01} = I_{Q2\_10} = I_{D1\_10} = I_{D2\_01} = 0 \tag{67}$$

Using Equations (16), (52)–(66) the rms values of the transistor, diode, and capacitor currents can be expressed as the following:

$$I_{Q1\_rms} = I_{Q2\_rms} = \sqrt{D(I_{L1} + I_{L2})^2} \tag{68}$$

$$I_{D1\_rms} = I_{D2\_rms} = \sqrt{D(I_{L1} + I_{L2})^2 + (1-2D)\left(I_{L1} - I_{C1_{disch}}\right)^2} \tag{69}$$

$$I_{D3\_rms} = I_{L2} = I_o \tag{70}$$

$$I_{C1\_rms} = \sqrt{(2D)(I_{L2})^2 + 2(1-D)\left(\frac{2D}{1-2D}I_{L2}\right)^2} \tag{71}$$

$$I_{C2\_rms} = \sqrt{2D(I_{L1} + I_{L2})^2} \tag{72}$$

$$I_{C3\_rms} = \sqrt{(1-2D)(I_{L2})^2 + D(I_{L1} - I_{C1\_disch} - I_{L2})^2 + D(I_{L1})^2} \tag{73}$$

$$I_{C4\_rms} = \sqrt{(1-2D)(I_{C1\_disch})^2 + 2D(I_{L2})^2} \tag{74}$$

2.7. Comparison with Other Multilevel Step-Up Converters

Based on the derived Equations (15), (21), and (26), which define the voltage gain and stress of the proposed converter, comparative analysis can be made between the proposed converter and other multilevel converters, as shown in Table 1. In this comparison, the proposed converter is compared with the conventional TLB converter, a three-level quasi-z-source (TL-QZS) converter in [9], and an input-parallel-output-series (IPOS) converter in [24].

The conventional TLB converter has an ideal voltage gain of 1/(1-*D*). The voltage stress across the semiconductor devices of the conventional TLB converter is $V_o/2$. In [9], this converter has a voltage gain of 2/(3-4*D*), and the voltage stress across the semiconductor devices is $V_o/2$. The duty cycle of this converter is limited between 50% and 75%, which makes the converter very sensitive to any change in duty. In [24], the converter discussed in this paper has a voltage gain of 2/(1-*D*), and the voltage stress across the power switches is $V_o/2$. Table 1 presents a peer-to-peer comparison between the proposed converter, the TL-QZS converter in [9], and the IPOS converter in [24].

Table 1. Comparisons between the proposed converter and other step-up solutions without magnetic coupling. TLB: three-level boost; TL-QZS: three-level quasi-z-source; and IPOS: input-parallel-output-series.

Header	Conventional TLB Converter	TL-QZS Converter in [9]	IPOS Converter in [24]	Proposed Converter
Voltage Gain	$\frac{1}{1-D}$	$\frac{2}{3-4D}$ $(0.5 \leq D < 0.75)$	$\frac{2}{1-D}$ $(0 \leq D < 1)$	$\frac{1+D}{1-D}$, $(0 < D < 0.5)$ $\frac{0.5+D}{1-D}$, $(D \geq 0.5)$
Voltage Stress	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2(1+D)}$, $(0 < D < 0.5)$ $\frac{V_o}{1+2D}$, $(D \geq 0.5)$
No. of Transistors	2	2	2	2
No. of Diodes	2	3	3	3
No. of Inductors	1	2	2	2
No. of Capacitors	2	4	3	4

Figure 6a,b show a comparison of the voltage gain *M* versus duty cycle *D* and the normalized voltage stress (V_s/V_o) versus *D* among the four converters, respectively. This comparison shows that the proposed converter has a higher voltage gain compared with the conventional TLB converter. The TL-QZS converter has a higher voltage gain compared with the proposed converter, but the main drawback for the TL-QZS converter is its limited operational range ($0.5 \leq D < 0.75$). The IPOS converter in [24] has the highest voltage gain; however, the proposed converter has the least voltage stress on the semiconductor devices, which means that it can be built using semiconductor devices with lower rated voltage, leading to higher efficiency, and a lower cooling system requirement and hence, higher power density.

From Equation (26), the stress voltage in the proposed converter depends on both V_o and *D*, and the stress voltage swings between 50% of V_o and 33.33% of V_o.

3. Component Parameters Design

3.1. Selection of the Semiconductor Devices

From Equations (15), (21), and (26), the voltage stress across the semiconductor devices depends on both the output voltage and the value of D, as depicted in Figure 7. The peak current flowing through Q_1 and Q_2 when the proposed converter is operating at $D < 0.5$ and $D > 0.5$ is the sum of the input and output currents. The peak current flowing through D_1 and D_2 when the proposed converter is operating at $D < 0.5$ and $D > 0.5$ is described by Equation (75). Equations (43) and (65) show the peak instantaneous current that flows through D_3.

$$I_{d1\_peak} = I_{d2\_peak} = \begin{cases} I_{L1} + I_{L2} & D < 0.5 \\ I_{L1} - I_{L2}\frac{2D-1}{2(1-D)} & D \geq 0.5 \end{cases} \quad (75)$$

With the growing advancements in the area of wide-bandgap (WBG) semiconductor devices, utilizing these devices in the proposed converter enhances the efficiency of the converter, leading to a reduction in the cooling system requirement, which in the end yields high-power density and high specific power. For diodes D_1, D_2, and D_3, silicon carbide (SiC) Schottky diodes can be utilized, because they have zero reverse recovery charges ($Q_{rr} = 0$), which alleviates the problem of the reverse recovery current that causes EMI problems. For Q_1 and Q_2, there are three major technologies available in the market for transistors, namely: SiC metal oxide field effect transistor (SiC MOSFET), gallium nitride (GaN) enhancement high-electron mobility transistor (E-HEMT), and GaN cascode HEMT. The lateral GaN HEMT is based on the piezoelectric effect between a layer of GaN and a layer of aluminum gallium nitride (AlGaN), which results in a two-dimensional (2-D) electron gas (2-DEG) layer between the drain (D) and source (S) of the GaN HEMT, which reduces the on-resistance of the device [25]. The GaN E-HEMT has the lowest on-resistance (R_{on}) and the lowest gate charge (Q_{GD}) compared with SiC MOSFETs and GaN cascode HEMTs. The driving of GaN E-HEMTS is very challenging, because they are very sensitive to the parasitics of the printed circuit board (PCB). The GaN cascode HEMT is composed of a high-voltage depletion GaN die and a low-voltage enhancement silicon (Si) MOSFET, and it does not have the driving circuit's problems as in the GaN E-HEMT, as the GaN cascode HEMT is driven like a typical Si MOSFET. The GaN cascode HEMT has a slightly higher R_{on} and Q_{GD} compared with the GaN E-HEMT; thus, if the power electronics designer can afford the time to optimize the PCB to minimize the power loop and the gate-to-source-loop parasitic inductances, the utilization of the GaN E-HEMT is recommended. In Table 2, a peer-to-peer comparison between three WBG transistors available in the market is presented. This shows that if the converter is built using GaN E-HEMTs, it will have lower conduction and switching losses.

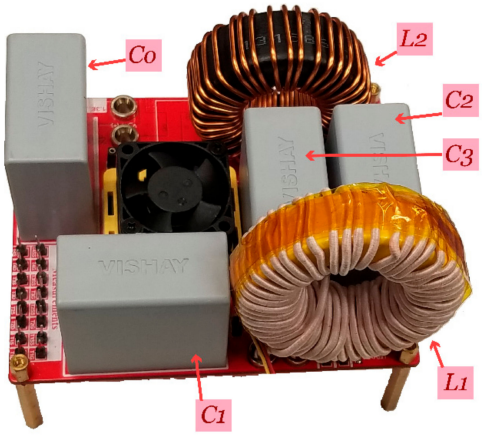

Figure 7. Experimental setup.

Table 2. Comparison between wide-bandgap (WBG) transistors available in the market.

Header	SCT2120AF	TPH3212PS	GS66508T
1-4			
Manufacturer	ROHM	Transphorm	GaN Systems
Semiconductor Material	SiC	GaN	GaN
Transistor Technology	MOSFET	Cascode HEMT	Enhancement HEMT
I_D Continuous	29 A	27 A	30 A
Device Package	TO220AB	TO-220	GaNPX-4
Switch Dimensions	-	15×10 mm^2	7×4.5 mm^2
R_{on}	120 mΩ	72 mΩ	55 mΩ
Q_{GD}	17 nC	14 nC	1.8 nC
Q_{rr}	53 nC	90 nC	0
Junction to Case Thermal Resistance	0.86 °C/W	1.2 °C/W	0.5 °C/W
Figure of Merit (Q_{GD} X R_{on})	2040	1008	99

3.2. Design of the Inductors

If the maximum allowed current ripples allowed for L_1 and L_2 are ΔI_{L1} and ΔI_{L2}, respectively, both inductors can be designed as follows. The inductances can be calculated in the charging state:

$$L_1 = \frac{\Delta T}{\Delta I_{L1}} \cdot V_{L1} \tag{76}$$

$$L_2 = \frac{\Delta T}{\Delta I_{L2}} \cdot V_{L2} \tag{77}$$

where ΔT is the charging time, which is T_{11} (when $D > 0.5$) and is T_{10} or T_{01} (when $D < 0.5$). The values of L_1 and L_2 can be determined using Equation (78) as follows:

$$L_1 = \text{or} L_2 = \begin{cases} \frac{D(0.5-D)}{\Delta I_L \, f_s(1-D)} V_{in} & D < 0.5 \\ \frac{(2D-1)(D-0.5)}{\Delta I_L \, f_s(1-D)} \, V_{in} & D > 0.5 \end{cases} \tag{78}$$

where f_s is the switching frequency, and ΔI_L can be ΔI_{L1} or ΔI_{L2}.

3.3. Design of the Capacitors

Assuming that the maximum allowed voltage ripples allowed for C_1, C_2, C_3, and C_4 are ΔC_1, ΔC_2, ΔC_3 and ΔC_4, respectively, the capacitances of these four capacitors can be calculated as follows, where ΔT can be the charging time or the discharging time. The following relationships define the correlation between the capacitors' ripple voltages and their capacitances.

$$\begin{cases} C_1 = \frac{\Delta T}{\Delta V_{C1}} I_{C1} \\ C_2 = \frac{\Delta T}{\Delta V_{C2}} I_{C2} \\ C_3 = \frac{\Delta T}{\Delta V_{C3}} I_{C3} \\ C_4 = \frac{\Delta T}{\Delta V_{C4}} I_{C4} \end{cases} \tag{79}$$

$$C_1 = \begin{cases} \frac{D \; I_o}{\Delta V_{C1} \, f_s} & D < 0.5 \\ \frac{(2D-1) I_o}{\Delta V_{C1} \, f_s} & D > 0.5 \end{cases} \tag{80}$$

$$C_2 = \begin{cases} \frac{D \; (I_{L1}+I_o)}{\Delta V_{C2} \, f_s} & D < 0.5 \\ (I_{L1} - \frac{2D-1}{2(1-D)} I_o)\left(\frac{1-D}{\Delta V_{C2} \, f_s}\right) & D > 0.5 \end{cases} \tag{81}$$

$$C_3 = \begin{cases} \frac{D\ I_o}{\Delta V_{C3}\ f_s} & D < 0.5 \\ \frac{(1-D)I_o}{\Delta V_{C3}\ f_s} & D > 0.5 \end{cases} \quad (82)$$

$$C_4 = \begin{cases} \frac{D\ I_o}{\Delta V_{Co}\ f_s} & D < 0.5 \\ \frac{(2D-1)I_o}{\Delta V_{C4}\ f_s} & D > 0.5 \end{cases} \quad (83)$$

4. Loss Analysis

The losses in the proposed converter can be divided into the following major contributors, namely: conduction and switching losses of the transistors Q_1 and Q_2, losses of the diodes D_1, D_2, and D_3, losses of the inductors (L_1 and L_2), and losses of the capacitors (C_1, C_2, C_3, and C_4).

4.1. Conduction and Switching Losses of Transistors

Because the rms currents flowing through Q_1 and Q_2 are the same, as shown in Equations (47) and (68), and assuming that both transistors have the same on-resistance, R_{on}, the total conduction loss of both Q_1 and Q_2 can be calculated by Equation (84) as follows

$$P_{tr\_cond} = 2 \cdot I_{Q1\_rms}^2 \cdot R_{on} \quad (84)$$

In a typical transistor, there are four major contributors to the switching loss, namely: (1) the overlap of the transistor current and voltage at the instant of turning on and off; (2) gate charge losses, which is caused by the charge stored in the gate capacitance; (3) the loss caused by the parasitic capacitance of the transistor, which is caused by the energy stored in C_{OSS} when the transistor is off; and (4) the loss caused by the reverse recovery charge of the body diode of the transistor (because the experimental work was implemented with GaN E-HEMTs, which do not have body diodes and have zero reverse recover charges, this loss component can be neglected). Equation (85) describes the total switching loss of the two transistors of the proposed converter, where f_s is the switching frequency, t_r and t_f are the rise and fall times of the transistor, respectively, Q_T is the gate charge, and V_G is the gate driver voltage. The drain-to-source voltage of the E-HEMTs equals half V_{C3} and is thus depicted as V_{C2}.

$$P_{tr\_sw} = 2 \cdot f_s \cdot \left(0.5 \cdot V_{c2} \cdot I_{Q1} \cdot \left(t_r + t_f\right) + 0.5 \cdot V_{C2}^2 \cdot C_{OSS} + Q_T \cdot V_G\right) \quad (85)$$

4.2. Diode's Losses

Because the experimental setup is implemented using SiC Schottky diodes, the reverse recovery switching loss of the diodes is neglected; however, the loss caused by the capacitive charge (Q_C) of the Schottky diodes is considered. The conduction loss of these diodes depends on the forward voltage and the rms currents flowing through the diodes. Equation (86) calculates the total losses of the three diodes of the proposed converter:

$$P_d = V_{fd} \cdot (2 \cdot I_{D1\_rms} + I_{D3\_rms}) + Q_C \cdot V_{C2} \cdot f_s \quad (86)$$

where V_{fd} and Q_C are the forward voltage and the total capacitive charge of the SiC diode, respectively.

4.3. Inductors' Losses

The inductors have two main loss components, namely the conduction loss, and the core loss. The conduction loss is caused by the dc current component flowing in the inductors' windings, while the core loss is caused by the inductors' ripple currents. The core loss equation should be provided by the core manufacturer. The inductors' total conduction loss, P_{L_cond}, can be calculated using

Equation (87), the inductors' core loss, P_{L_core}, can be calculated using Equation (88), and the total losses in the inductors, P_{L_tot}, can be calculated using Equation (89).

$$P_{L\_cond} = I_{L1}^2 \cdot R_{L1} + I_{L2}^2 \cdot R_{L2} \tag{87}$$

where R_{L1} and R_{L2} are the series parasitic resistances of L_1 and L_2, respectively.

$$P_{L\_core} = \frac{f}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.65}}} + \left(\mathrm{df}^2\mathrm{B}^2\right) \tag{88}$$

Equation (88) is provided by "Micrometals" (the manufacturer of the inductor cores used in the experimental prototype), where the equation's parameters can be derived from the datasheet of each specific core size and dimension:

$$P_{L\_tot} = P_{L\_core} + P_{L\_cond} \tag{89}$$

4.4. Capacitors' Losses

The losses of the capacitors in the proposed converter are calculated as the conduction loss of these capacitors caused by their equivalent series resistance (ESR). The power loss of the four capacitors of the proposed converter, P_C, is expressed by Equation (90), where ESR_{C1}, ESR_{C2}, ESR_{C3}, and ESR_{C4} are the equivalent series resistances of the four capacitors.

$$P_C = I_{C1\_rms}^2 \cdot ESR_{C1} + I_{C2\_rms}^2 \cdot ESR_{C2} + I_{C3\_rms}^2 \cdot ESR_{C3} + I_{C4\_rms}^2 ESR_{C4} \tag{90}$$

5. Experimental Results and Analysis

A scaled-down experimental prototype was built, as shown in Figure 7, in order to validate the proposed converter topology and its theoretical analysis. In this experimental work, the fuel cell is depicted by a dc-voltage source. The converter is controlled by a TMS320f28377s microcontroller, and the currents are sensed by a hall-effect current transducer ACS730KLCTR-40AB-T. The power circuit is constructed using GS66508T E-HEMTs (rated voltage is 650 V, and rated current is 30 A) and C3D10065E SiC Schottky diodes (rated voltage is 650 V, and rated current is 32 A). The switching frequency, f_s, is 100 kHz, and the values of the two inductors L_1 and L_2 are 350 µH and 250 µH, respectively. The capacitors C_1, C_2, C_3, and C_4 have the same value (capacitance = 80 µF, and rated dc-voltage = 700 V). The load is represented by a 120 Ω resistance, R_L. The main experimental parameters of the proposed converter prototype are shown in Table 3.

In this experimental work, two case studies are investigated:

(1) Case study I: V_{in} = 200 V, D = 0.3, R_L = 120 Ω; and
(2) Case study II: V_{in} = 100 V, D = 0.7, R_L = 120 Ω

The experimental results of case study I are intended to verify the theoretical analysis of the converter when $D < 0.5$ and are presented in Figure 8, while the experimental results of case study II are intended to verify the theoretical analysis of the converter when $D > 0.5$ and are presented in Figure 9.

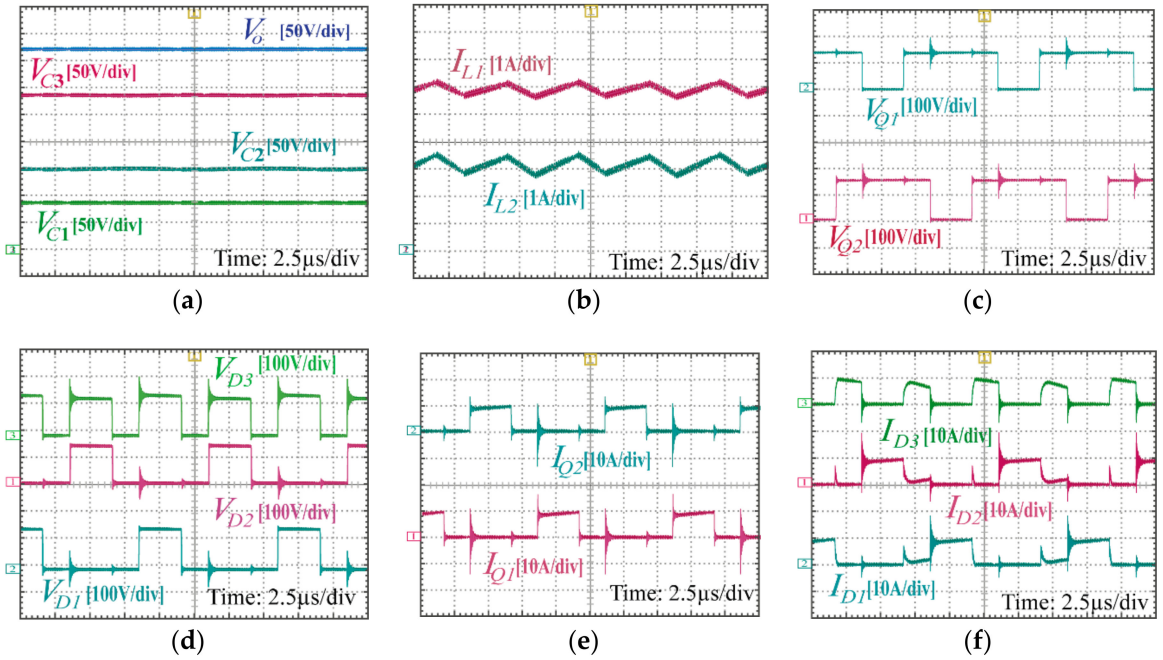

Figure 8. Experimental results when V_{in} = 200 V, D = 0.3, R_L = 120 Ω, P_{out} = 1.15 kW.

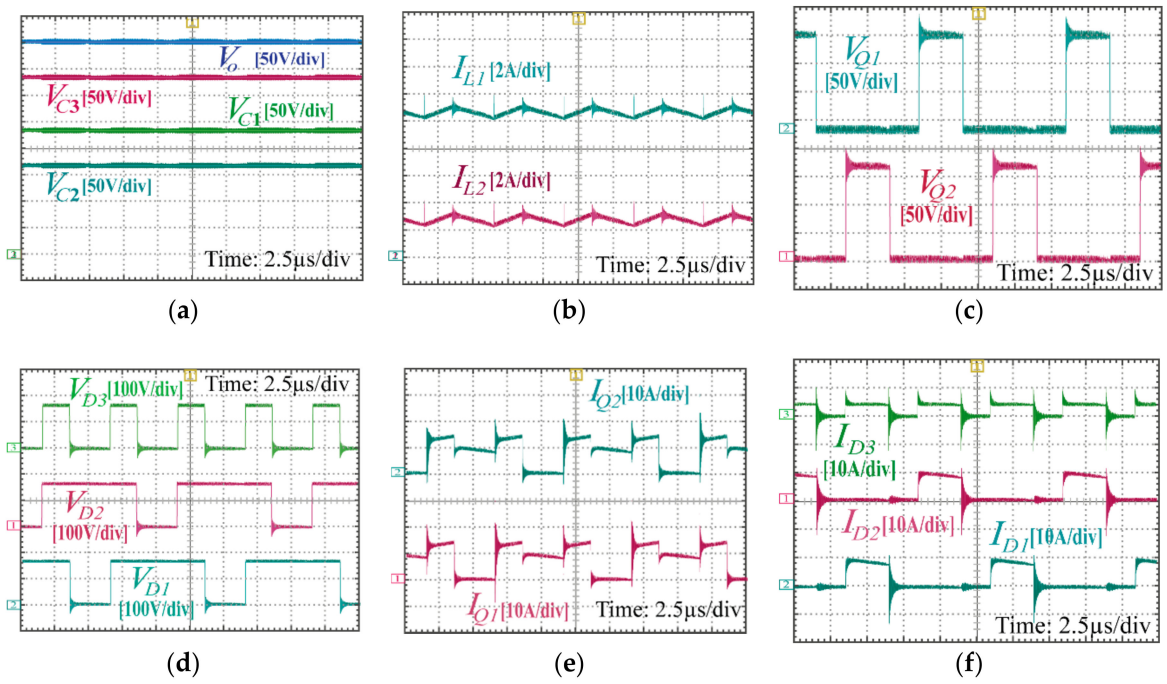

Figure 9. Experimental results when V_{in} = 100 V, D = 0.7, R_L = 120 Ω, P_{out} = 1.3 kW.

5.1. Case Study I (D = 0.3, V_{in} = 200 V, R_L = 120 Ω)

When D is less than 0.5, Equations (18), (20), and (24) describe the four capacitors' voltages, and hence, they can be calculated as the following: V_{C1} = 85.7 V, V_{C2} = 142.9 V, V_{C3} = 285.7 V, and V_o = 371.4 V. Figure 8a validates these findings. The two inductor currents, I_{L1} and I_{L2}, are shown in Figure 8b, and the frequency of the ripple currents is 200 kHz, which is double the switching frequency. The currents flowing through the two inductors I_{L1} and I_{L2}, are close to 5.5 A and 3 A, respectively, which comply with the theoretical Equations (64) and (70). The voltage stresses across the E-HEMTs (Q_1 and Q_2) and the diodes (D_1, D_2, and D_3) are shown in Figure 8c,d, respectively, where the voltage

stresses swing between 0 V and 140 V (=V_{C2}), which comply with Equation (26). Figure 8e,f show the currents flowing through the E-HEMTs, and the diodes, where the currents of (Q_1, Q_2, D_1, and D_2) swing between 0 A and 9 A, which comply with Equations (66) and (67). Also, Figure 8e shows I_{D3}, where D_3 conducts only when both Q_1 and Q_2 are off, and the magnitude of I_{D3} during conduction is close to 7.5 A, which complies with Equation (65). It is worth noting that the semiconductor devices should be selected with higher rated voltage and current to assure operating in the safe operation area (SOA) of these devices and account for the voltage spikes (caused by the parasitic inductance of the PCB) and current spikes (caused by the parasitic capacitance of the SiC Schottky diodes).

5.2. Case Study II (D = 0.7, V_{in} = 100 V, R_L = 120 Ω)

From Equations (11), (15), and (24), the voltage across the four capacitors can be calculated as follows: V_{C1} = 233.33 V, V_{C2} = 166 V, V_{C3} = 333 V, and V_o = 400 V. These findings are verified by Figure 9a. Figure 9b shows the currents flowing through the two inductors, I_{L1} and I_{L2}, which have ripple currents with frequencies equal to double the switching frequency of the converter (the periodic time of the ripple currents = 5 μS, and the periodic time of the switching = 10 μS). From Figure 9b, I_{L2} is close to 3.3 A, and I_{L1} is close to 13 A, which verify Equations (40) and (42). Figure 9c,d show the voltage stress across the E-HEMTs (Q_1 and Q_2) and the diodes (D_1, D_2, and D_3), respectively, where the voltage stress swings between 0 V and 166 V, namely between 0 V and half the voltage across C_3, which verifies Equation (26). The currents of the E-HEMTs (Q_1 and Q_2) are shown in Figure 9e; each current swings between three levels, 0 A (the E-HEMT is off, and the other one is on), 11 A (the E-HEMT is on, and the other one is off), and 16 A (both of the E-HEMTs are on), which verify Equations (37), (44), and (45).

Figure 9e,f show the currents flowing through the diodes (D_1, D_2, and D_3). From Equations (45) and (46), diode D_1 conducts only when S_1S_2 = {01}, while diode D_2 conducts only when S_1S_2 = {10}, and the magnitude of the current flowing during conduction = $I_{L1} - ((2D - 1)\, I_{L2}/(2D - 2))$ = 11 A, which is verified by Figure 9f. Figure 9e shows that D_3 conducts only when either of the E-HEMTs is off, and the current flowing during conduction is close to 6 A, which verifies Equation (43).

5.3. The Loss Analysis of the Proposed Converter

Using Equations (84)–(90), the losses of the proposed converter can be calculated for any value of V_{in}, D, and R_L. The converter losses for case studies I and II are investigated and analyzed. Figure 10 shows the loss distributions for the proposed converter for both case study I and case study II.

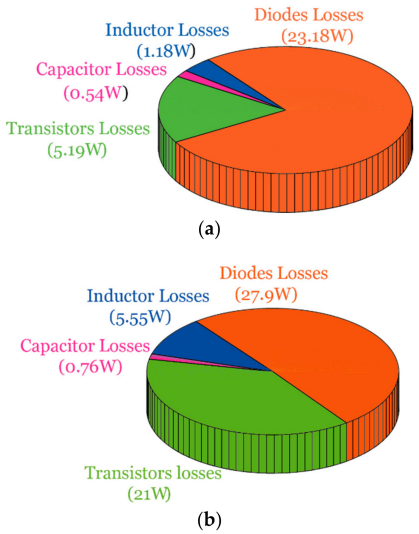

Figure 10. Calculated loss distributions for the experiment (**a**) When V_{in} = 200 V, D = 0.3, and R_L = 120 Ω. (**b**) When V_{in} = 100 V, D = 0.7, and R_L = 120 Ω.

Table 3. Main Experimental Parameters of the Proposed Converter.

Components and Parameters	Values
Output power (P_{out})	1.15 kW, 1.3 kW
Input dc-voltage (V_{in})	200 V, 100 V
Switching frequency (fs)	100 kHz
Inductor (L_1)	350 µH
Inductor (L_2)	250 µH
Capacitors (C_1, C_2, C_3, C_4)	80 µF, 700 V
E-HEMTs (Q_1, Q_2)	GS66508T (from GaN Systems)
Diodes (D_1, D_2, D_3)	C3D10065E (from Cree)
Load (R_L)	120 Ω

Figure 10a shows the loss distributions when $D = 0.3$, $V_{in} = 200$ V, and $R_L = 120$ Ω, $P_{out} = 1.15$ kW. The total losses of the converter in this case study equal 27.16 W, and the efficiency of the converter equals 97.6%. The main contributor of losses in this case is the diodes (85.3% of total losses), because of their relatively high forward voltage (V_{fd}) = 1.8 V. The total losses of the E-HEMTs are 19% of the total losses, and this is because of their low on-resistance and zero reverse recovery charges. The losses of the inductors and capacitors account for 4.3% and 2.8% of the total losses of the proposed converter, respectively.

Figure 10b shows the loss distributions when $D = 0.7$, $V_{in} = 100$ V, and $R_L = 120$ Ω, $P_{out} = 1.333$ kW. The total losses of the converter in this case study equal 55.21 W, and the efficiency of the converter equals 95.86%. The main contributor of losses in this case is also the diodes (50.5% of total losses). The total losses of the E-HEMTs are 38% of the total losses. The losses of the inductors and capacitors account for 10% and 1.37% of the total losses of the proposed converter, respectively.

The efficiency curves of the proposed converter that depict the efficiency at different power levels are shown in Figure 11, and they were obtained from the experimental setup ($V_{in} = 100$ V, $f_s = 100$ kHz, $R_L = 120$ Ω). The efficiency is depicted by two curves, one for operation when $D < 0.5$, and the other one for operation when $D \geq 0.5$.

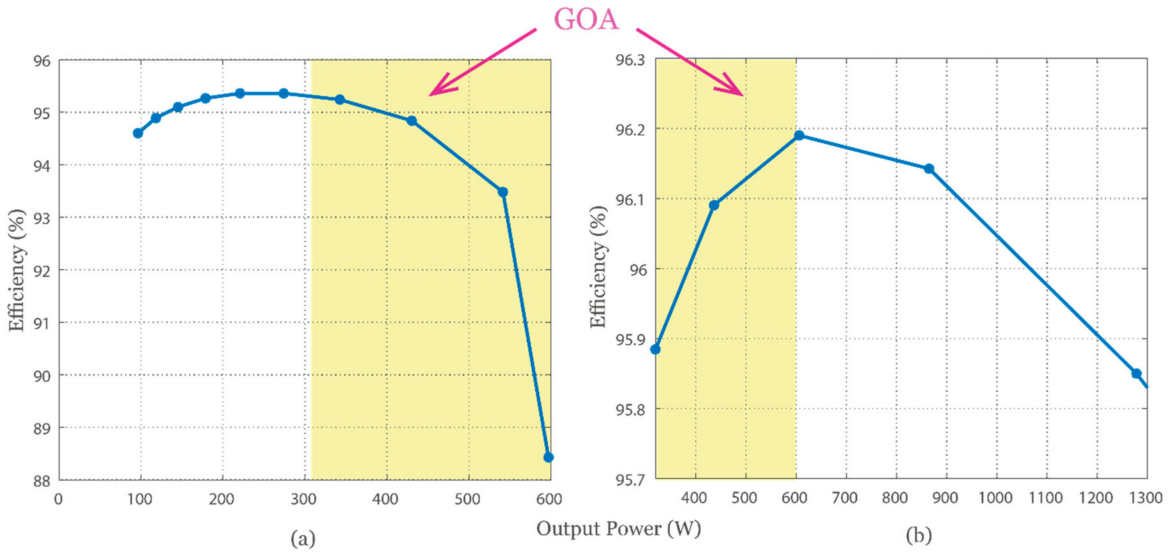

Figure 11. Efficiency curves of the proposed converter ($V_{in} = 100$ V, $R_L = 120$ Ω) (**a**) When $D < 0.5$. (**b**) When $D \geq 0.5$.

In the GOA, the same voltage gain (M) can be achieved by two different values of D; one of them is less than 0.5, and the other one is greater than 0.5. Figure 12 shows the calculated efficiency

of the proposed converter in the GOA. When V_{in} = 100 V and R_L = 120 Ω, one curve presents the efficiency versus M when D is less than 0.5, while the other curve shows the efficiency versus M when D is greater than 0.5. From Figure 12, it is obvious that if the desired M is in the GOA ($2 < M < 3$), the efficiency of the proposed converter is higher when D is selected to be higher than 0.5.

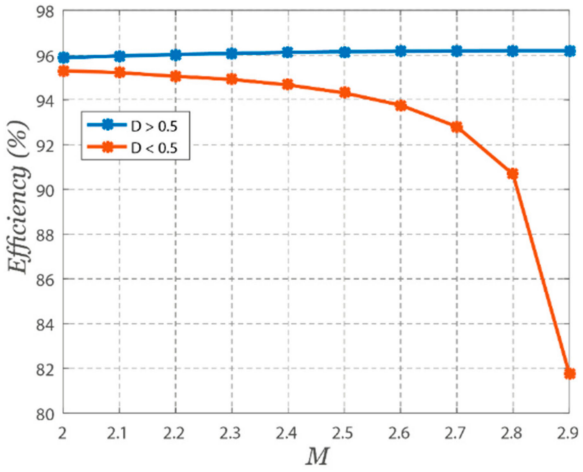

Figure 12. Calculated efficiency curves in the GOA (V_{in} = 100 V, R_L = 120 Ω).

6. Conclusions

A new three-level boost (TLB) converter based on a flying-capacitor switching network and an integrated LC^2D output network was introduced and presented. It can be used as an interface between the fuel cells and the dc-link bus of the three-phase inverter in an EV powertrain. It has several advantages of continuous input current, extended voltage gain, lower voltage stress on the semiconductor devices, common ground between the input and output ports, and a wide voltage gain range. These features render the proposed converter an excellent solution for the soft output characteristics of the fuel cells. The steady state analysis of the proposed converter under the continuous conduction mode (CCM) was investigated. The voltage gain, the voltage stress on the semiconductor devices, and the number of the semiconductor devices and passive components of the proposed converter were compared with other three-level step-up solutions, and the importance of the proposed converter was verified experimentally. The proposed converter was built using GaN E-HEMTs and SiC Schottky diodes, and the experimental results validated the theoretical analysis.

Author Contributions: N.E. developed the proposed topology, analyzed it, and built it. H.M. Helped in the prototype development, and analysis. O.M. is the main supervisor who leads the project, identifies the ideas, checks the results and edits the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

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