Constant Voltage Constant Current Control for Stable Operation of DC–DC Converters in Multilevel Inverters

Ahmed Ali[1], Ahmad Asrul Ibrahim[1], Praveen Kumar Balachandran[2,3,*], Mohd Amran Mohd Radzi[4], Samir Salem Al-Bawri[5] and Muhammad Ammirrul Atiqi Mohd Zainuri[1]

[1] Department of Electrical, Electronic, and System Engineering, Universiti Kebangsaan Malaysia, Bangi, Malaysia

[2] Department of Electrical and Electronics Engineering, Vardhaman College of Engineering, Hyderabad, India

[3] Department of Electrical and Electronics Engineering, Chennai Institute of Technology, Chennai, India

[4] Department of Electrical and Electronic Engineering, Universiti Putra Malaysia, Serdang, Malaysia

[5] Space Science Centre, Institute of Climate Change, Universiti Kebangsaan Malaysia (UKM), Bangi, Malaysia

INFORMATION

Keywords:
DC-DC converters
DC-link voltage
multilevel inverters (MLIs)
voltage regulation
light-load conditions

DOI: 10.23967/j.rimni.2026.10.77288

SCIPEDIA Revista Internacional de Métodos Numéricos para Cálculo y Diseño en Ingeniería

Revista Internacional Métodos numéricos para cálculo y diseño en ingeniería RIMNI

In cooperation with CIMNE

Constant Voltage Constant Current Control for Stable Operation of DC–DC Converters in Multilevel Inverters

Ahmed Ali[1], Ahmad Asrul Ibrahim[1], Praveen Kumar Balachandran[2,3,*], Mohd Amran Mohd Radzi[4], Samir Salem Al-Bawri[5] and Muhammad Ammirrul Atiqi Mohd Zainuri[1]

[1]Department of Electrical, Electronic, and System Engineering, Universiti Kebangsaan Malaysia, Bangi, Malaysia

[2]Department of Electrical and Electronics Engineering, Vardhaman College of Engineering, Hyderabad, India

[3]Department of Electrical and Electronics Engineering, Chennai Institute of Technology, Chennai, India

[4]Department of Electrical and Electronic Engineering, Universiti Putra Malaysia, Serdang, Malaysia

[5]Space Science Centre, Institute of Climate Change, Universiti Kebangsaan Malaysia (UKM), Bangi, Malaysia

ABSTRACT

Multilevel inverters (MLIs) offer superior waveform quality, reduced harmonic distortion, and lower voltage stress compared to conventional two-level converters. In such systems, the individual voltage levels are typically generated through DC-DC converters, where each level is produced for a specific duration by selectively connecting one or more DC sources. To generate lower voltage levels, some DC sources are temporarily disconnected, resulting in light-load or no-load conditions making the output of the DC-DC converters unstable. Most existing control strategies for DC-DC converters are designed to regulate the output voltage assuming a continuously connected load, which leads to instability when the converter operates at light or no-load conditions. To address this challenge, this paper employs a Constant Voltage Constant Current (CVCC) control method to ensure stable voltage generation for MLI voltage levels. The proposed method is benchmarked against Proportional–Integral (PI), Fuzzy Logic (FL), and Sliding Mode Control (SMC) techniques. Simulation results demonstrate that the proposed method achieves superior voltage stability, accuracy, and transient performance. The proposed method is used to generate three-level and seven-level voltage waveforms in the PLECS environment, and its real-time implementation further validates its effectiveness and practical applicability. The results confirm excellent voltage regulation, with capacitor voltage fluctuations remaining below 1 V (corresponding to only 0.33% of the nominal 300 V DC-link voltage, compared to the commonly accepted ±5% tolerance).

OPEN ACCESS

Received: 06/12/2025

Accepted: 05/03/2026

Published: 29/05/2026

DOI
10.23967/j.rimni.2026.10.77288

Keywords:
DC-DC converters
DC-link voltage
multilevel inverters (MLIs)
voltage regulation
light-load conditions

1 Introduction

DC-DC converters are fundamental components in power electronics, used extensively to regulate voltage levels in various applications [1–3]. Achieving precise and stable output voltage is crucial

*Correspondence: Praveen Kumar Balachandran (praveenbala038@gmail.com).

for many applications, necessitating effective closed-loop control strategies. The diverse closed-loop voltage control methods employed in DC-DC converters can be classified into two main categories, namely linear and non-linear techniques [4,5].

Linear control techniques are the earliest methods applied to control the output voltage of DC-DC converters. Among the most common strategies employed are Proportional-Integral (PI) control [6], Proportional-Integral-Derivative (PID) control [7], voltage mode control, and current mode control; each has been used to maintain precise and reliable output voltage in various applications [8–11]. While PI controllers are easy to implement and improve the performance by removing the steady-state error. However, they can struggle with transient response, as they lack the predictive capability provided by the derivative term found in PID controllers. To overcome this limitation derivative term is added, which predicts the future errors to enhance stability. The tuning of PID parameters, proportional gain, integral gain, and derivative gain, is crucial for optimizing performance, with various methods available for this purpose. Voltage mode control regulates output voltage by adjusting the duty cycle based on feedback from the output voltage [12], offering simplicity and cost-effectiveness but potentially struggling under rapidly changing load conditions due to its reliance on average output voltage rather than instantaneous current feedback. To address these limitations, some designs incorporate additional filtering or hybrid approaches that combine voltage mode with current mode control. Current mode control enhances converter performance by incorporating feedback from both output voltage and inductor current, allowing for improved transient response and inherent overcurrent protection [13–15]. This method can be implemented in peak or average forms; peak current mode control limits maximum inductor current during switching cycles to prevent overcurrent conditions [16–18], while average current mode control smoothens fluctuations by averaging current over multiple cycles [19,20]. Each of these linear control techniques offers distinct advantages suited to specific operational requirements, while robustness remains the most significant issue, as these techniques have limitations in dealing with nonlinearities and uncertainties inherent in DC-DC converters. Their performance can degrade significantly under large disturbances or parameter variations. Moreover, the design and tuning of these controllers often require extensive simulations and experimental adjustments [21,22]. However, many studies have focused on optimal tuning of PI and PID controllers for DC converters using various techniques, including Ziegler-Nichols tuning [23,24], and genetic algorithms [25,26], but these enhancements often increase the complexity of the control design process. To overcome the limitations of linear controllers, various nonlinear control techniques have been explored for DC-DC converters. These methods offer better robustness to disturbances and uncertainties, achieving improved transient response and steady-state error.

Nonlinear control techniques play a crucial role in enhancing the performance and addressing the disturbances, uncertainties, and nonlinearities inherent in DC-DC converters, Sliding Mode Control (SMC) is a robust strategy that forces system states to adhere to a predefined sliding surface, ensuring stability despite variations in system parameters or external disturbances [27–29]; it excels in managing nonlinearities and can significantly improve voltage regulation by adjusting the duty cycle based on output voltage feedback. However, the chattering phenomenon [30,31], a high-frequency oscillation in the control signal, can be problematic and needs mitigation techniques such as the super twisting algorithm. Additionally, the design of the sliding surface can be challenging and may require precise tuning to ensure stability, especially for high-order systems. Hysteresis Control offers a simpler approach by employing a defined hysteresis band around the desired output voltage [32,33]; it rapidly switches the converter on and off to maintain output within this band, resulting in quick responses to load changes, although it may incur switching losses if not carefully tuned. Fuzzy Logic Control is another approach utilizes fuzzy set theory to handle uncertainties and nonlinearities without requiring

precise mathematical models [34,35]; it adapts to varying conditions through rule-based reasoning, making it particularly effective in applications where traditional control methods may struggle. Their performance heavily relies on the quality of the fuzzy rules and membership functions defined by the designer. Designing these rules can be complex, and improper tuning may lead to suboptimal performance or instability in dynamic conditions. Adaptive Control continuously adjusts its parameters based on real-time feedback from the system, allowing it to maintain robust performance under dynamic operating conditions, which is essential for converters facing unpredictable loads or input variations. However, they require sophisticated implementations and may be sensitive to modelling inaccuracies. If not properly managed, this sensitivity can lead to instability or degraded performance. Neural Network Control [36,37] leverages artificial intelligence to model complex relationships within power systems; neural networks can learn from past data and adapt their control strategies accordingly, improving response times and overall efficiency. Training neural networks and overfitting are remarkable limitations that make this approach undesirable in some applications. Model Predictive Control (MPC) is an advanced technique that predicts future system behaviour based on current states and inputs, optimizing control actions over a defined horizon while considering constraints [38,39]; this foresight allows MPC to effectively manage the nonlinear dynamics of buck converters, but its computational demands can be high, requiring high-performance processors. Backstepping Control [40] is another prominent approach that systematically designs a control law by breaking down the system into manageable subsystems, ensuring stability through recursive design; it is particularly useful for systems with complex dynamics. However, the complexity of backstepping control increases with the number of subsystems and interactions within highly nonlinear systems. This complexity can make implementation challenging and may require detailed knowledge of system dynamics. Passivity-Based Control (PBC) [41] focuses on energy-based methods to ensure system stability by designing controllers that maintain the passivity properties of the system, which can be advantageous in regulating energy flows within converters. PBC requires precise modelling of system dynamics; if there are significant uncertainties or disturbances, its effectiveness may diminish. Additionally, implementing PBC can be more complex compared to traditional control methods due to its reliance on energy considerations. Each of these nonlinear control techniques offers unique strengths that cater to specific challenges in the operation of DC-DC converters, contributing to improved performance, efficiency, and reliability across various applications.

All the above-mentioned linear and nonlinear control techniques have been extensively validated under nominal or moderate load conditions, where sufficient current ensures stable energy transfer and effective loop regulation. However, when subjected to light-load or no-load conditions, many of these methods exhibit degraded voltage regulation performance. Under extremely low current demand, the converter frequently operates in discontinuous conduction mode (DCM) [42,43], where the inductor current falls to zero and energy transfer becomes intermittent. In this regime, conventional control loops may lose effective regulation authority, resulting in voltage drift, overshoot, oscillations, or even instability. Consequently, maintaining stable voltage under very low load conditions remains a significant challenge for traditional control strategies.

1.1 Research Gap

Despite the considerable advancements in both linear and nonlinear control approaches, a fundamental limitation persists under light-load and no-load operation. Most conventional controllers are not explicitly designed to manage DCM behaviour or intermittent energy transfer, which becomes particularly problematic in applications requiring strict voltage stability. To address these challenges, alternative approaches such as pulse skipping modulation (PSM) have been proposed

[44]. PSM improves efficiency and stability by selectively skipping switching pulses when the load demand is minimal, thereby preventing excessive switching activity and maintaining output voltage within acceptable limits. This technique ensures that the converter avoids instability at no-load and light-load conditions, reduces unnecessary switching losses, and extends the overall lifetime of the power converter. However, it has several notable limitations that constrain its application in high-performance converters. Its variable switching frequency complicates filter design and makes meeting EMI requirements more difficult. The burst-mode operation also increases output voltage ripple, which is unsuitable for systems requiring tight regulation. In addition, PSM often relies on multiple digital components for detection and control, increasing implementation complexity. It also exhibits poor transient response because the converter may remain inactive during skipped cycles, delaying its reaction to sudden load changes. Finally, due to these drawbacks and the difficulty in achieving EMC/EMI compliance, PSM is generally restricted to low-power and non-critical applications.

1.2 Objective and Contribution

In the case of multilevel inverters (MLIs), the DC-DC converters responsible for generating the individual voltage levels are not continuously connected but are instead disconnected for certain intervals during operation. This intermittent connection can lead to voltage deviations from their predefined reference values, thereby affecting the stability and quality of the inverter output. Consequently, a stable and efficient control method is required to ensure that the voltage levels are properly maintained despite these disconnections. To address this issue, the present manuscript employs the constant voltage constant current control approach and demonstrates its applicability within the framework of MLIs, ensuring stable voltage regulation and improved overall system performance. The proposed CVCC control strategy should not be confused with the conventional Constant-Current Constant-Voltage (CCCV) algorithm used in battery charging systems. In CCCV charging, the controller operates sequentially: the system first regulates current (CC mode) until a voltage threshold is reached, and then switches to voltage regulation (CV mode) [45,46]. However, the proposed CVCC method regulates both current and voltage simultaneously through a dual-loop structure. It is specifically designed for DC-link capacitor dynamic voltage regulation in DC–DC converters supplying multilevel inverters, ensuring controlled energy flow and voltage stability under light-load, no-load, and intermittent operating conditions. Thus, unlike battery-oriented CCCV schemes, the proposed approach is not based on mode switching but on concurrent regulation to maintain stable converter performance.

The remainder of this manuscript is organized as follows: Section 2 presents the motivation of this work. Section 3 introduces the converter model, while Section 4 describes the proposed method in detail. Section 5 provides the simulation setup and results, followed by Section 6, which discusses the obtained results and highlights key findings. Finally, Section 7 concludes the manuscript with a summary of contributions and potential directions for future work.

1.3 Motivation

Fig. 1 illustrates a DC–DC converter operating with an intermittent load. The output voltage across the load is intended to remain constant while the load is connected. However, once the load is disconnected, the voltage across the capacitor becomes unstable, resulting in undesirable fluctuations. Furthermore, most of the methods reported in the literature assume continuous load presence, which limits their effectiveness under intermittent load conditions.

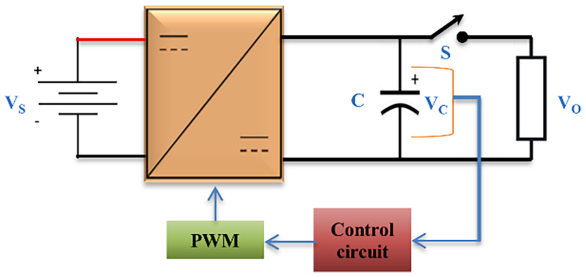


Figure 1: A DC-DC converter with an intermittent load

Fig. 2 represents the status of the switch (S) alongside the desired capacitor voltage. The primary objective is to develop a control circuit capable of maintaining a constant, ripple-free voltage across the capacitor under varying operating conditions, including both full-load and no-load conditions.

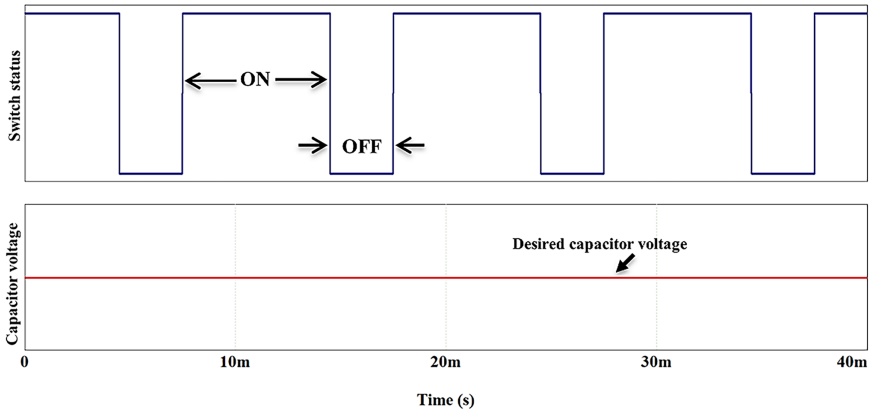


Figure 2: Switch status with the desired capacitor voltage

DC–DC converters are widely used in various power electronic applications. One of their key roles is to regulate and maintain a constant voltage across the capacitors in Multilevel Inverters (MLIs) as shown in Fig. 3. However, a major challenge arises when the inverter switches are turned off. In such conditions, the DC–DC converter becomes disconnected, leaving the capacitor voltage unregulated. As a result, the capacitor experiences instability and undesirable voltage fluctuations, which can degrade the inverter's performance and overall system reliability.

2 Converter Model

A DC–DC boost converter steps up the input dc voltage (V_s) to a higher voltage level (V_o), i.e., ($V_o > V_s$). A schematic diagram of a boost converter is depicted in Fig. 4. It consists of a source voltage (Vs), a controlled switch (Sw), a diode (D), a filter inductor (L), a filter capacitor (C), and an intermittent load. It is worth noting that the MOSFET (S_W) is running at a high switching frequency (f_s) while the auxiliary switch (S_A) connected in series with the load is working at a slow frequency (f) shown in Fig. 5. Where $f_s >> f$.

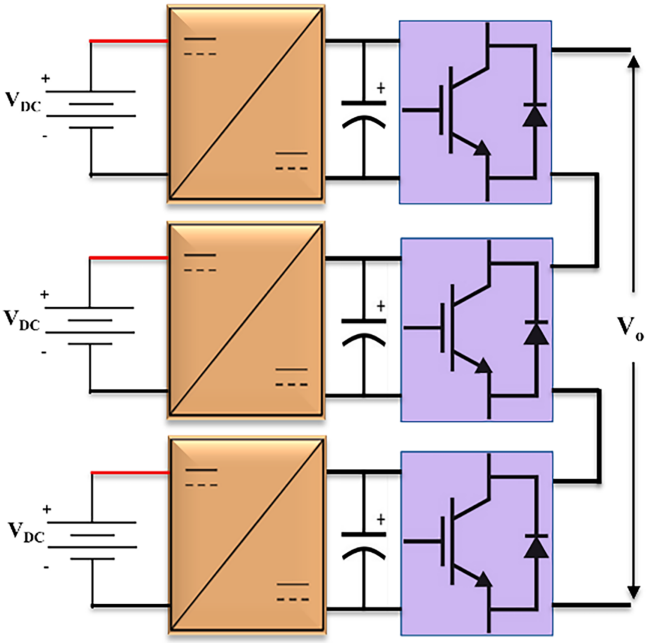


Figure 3: A multilevel inverter with DC-DC converters

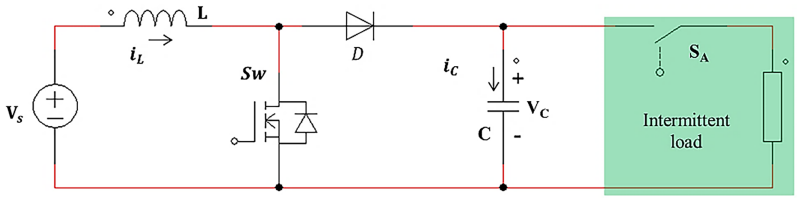


Figure 4: A DC-DC boost converter

Figure 5: Switching pattern of the main switch (S_W) and the load switch (S_A)

2.1 Converter Operating Modes

A converter with an intermittent load has five operating modes: two when the load is connected and three with a disconnected load. A detailed explanation of the four cases is provided in this section.

2.1.1 *Case I: When the Load Is Connected*

This is the normal case where the load is connected, the converter components are selected to meet the load requirements, such as capacitor voltage ripples, inductor current ripples, semiconductor devices ratings, etc. The analysis in this case is trivial, as given in the literature.

Mode I: Switch Closed

When the switch is closed, the diode is reverse-biased. Kirchhoff's voltage law around the path containing the source, inductor, and closed switch is

$$V_L = V_S = L\frac{di_{L(1)}}{dt} \tag{1}$$

The rate of change of current is a constant, so the current increases linearly while the switch is closed, as shown in Fig. 6. The change in inductor current is computed from

$$\frac{\Delta i_{L(1)}}{\Delta t} = \frac{\Delta i_{L(1)}}{DT} = \frac{V_S}{L} \tag{2}$$

Solving for Δi_L for the switch closed,

$$\Delta i_{L(1)} = \frac{V_S DT}{L} \tag{3}$$

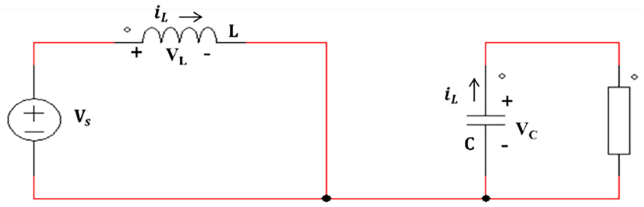


Figure 6: Equivalent circuit for the switch closed

Mode II: Switch Open

When the switch is opened, the inductor current cannot change instantaneously, so the diode becomes forward-biased to provide a path for the inductor current, as shown in Fig. 7. Assuming that the output voltage V_C is a constant, the voltage across the inductor is

$$\frac{\Delta i_{L(2)}}{\Delta t} = \frac{V_S - V_C}{L} \tag{4}$$

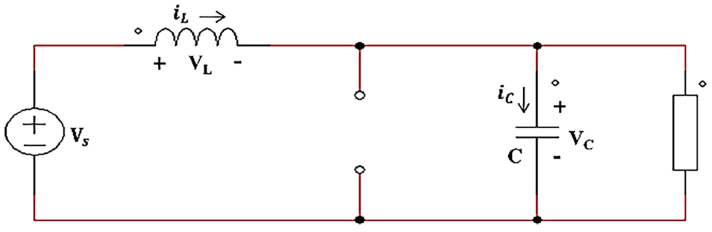


Figure 7: Equivalent circuit for the switch opened

The rate of change of inductor current is a constant, so the current must change linearly while the switch is open. The change in inductor current while the switch is open is

$$\frac{\Delta i_{L(2)}}{\Delta t} = \frac{\Delta i_{L(2)}}{(1-D)T} = \frac{V_S - V_C}{L} \tag{5}$$

Solving for Δi_L,

$$\Delta i_{L(2)} = \frac{(V_S - V_C)(1-D)T}{L} \tag{6}$$

Under steady-state operation, the average inductor voltage must be zero for periodic operation. Expressing the average inductor voltage over one switching period,

$$V_S D + (V_S - V_C)(1-D) = 0 \tag{7}$$

$$V_C = \frac{V_S}{1-D} \tag{8}$$

The inductor voltage and current waveforms are shown in Fig. 8.

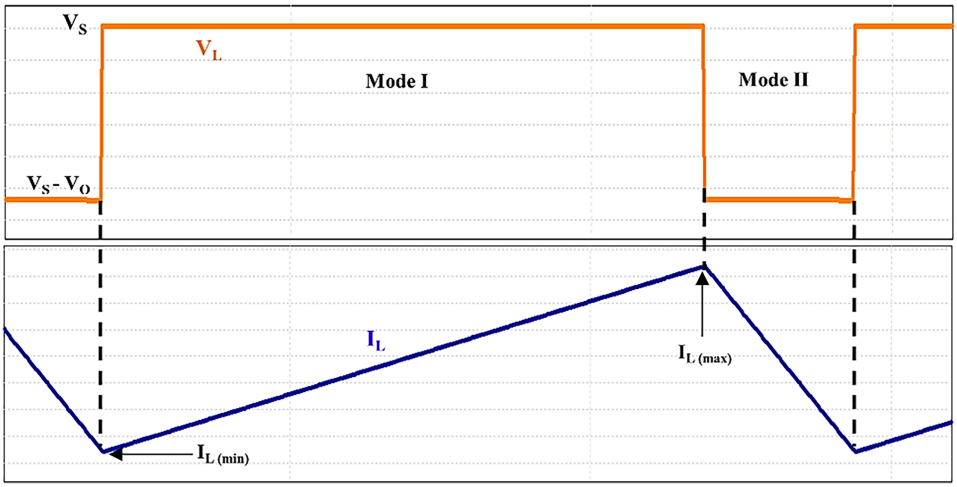


Figure 8: Inductor voltage and current waveforms during modes I and II

2.1.2 Case II: When the Load Is Disconnected

In this situation, at the moment the load is disconnected, the converter has three modes as explained below.

Mode I: Active Switch (S_W)

In this mode, immediately after the load is disconnected, the inductor current continues to charge the capacitor, whose voltage is slightly below the reference level. During this interval, the switch remains active and keeps toggling between the ON and OFF states; therefore, the average inductor current remains unaffected. By the end of this mode, once the capacitor voltage surpasses the threshold, the main switch is deactivated. The equivalent circuits corresponding to this mode are illustrated in Fig. 9a,b.

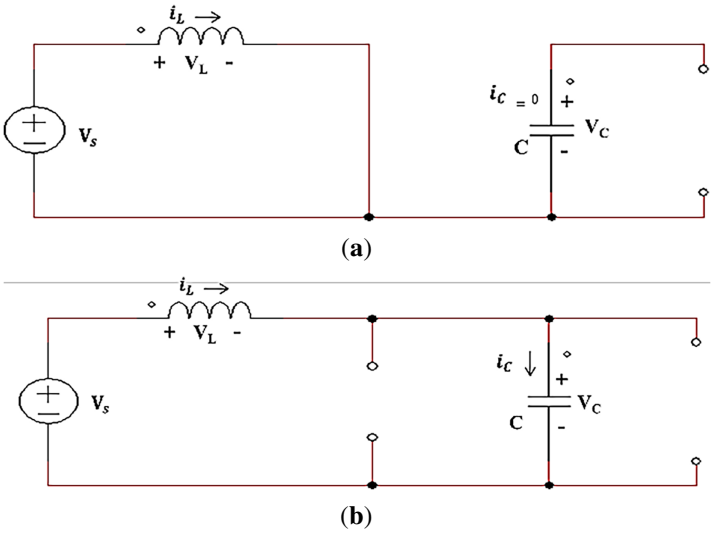


Figure 9: (a) Equivalent circuit for mode I for closed switch. (b) Equivalent circuit for mode I for open switch

In Fig. 9a, when the switch is closed, the expression of the inductor current is identical to that obtained when the load is connected. However, since the load is disconnected, the capacitor does not discharge. The inductor current and capacitor voltage variations can be expressed as:

Switch ON (duration dT_s, diode OFF):

$$L\frac{di_L}{dt} = V_s \tag{9}$$

$$C\frac{dv_C}{dt} = -i_o \approx 0 \tag{10}$$

In Fig. 9b, when the switch is open, the inductor current continues to charge the capacitor. Accordingly, both voltage across the capacitor and inductoe current can be written as:

Switch OFF (duration $(1-d)T_s$, diode ON):

$$L\frac{di_L}{dt} = v_s - v_C \tag{11}$$

$$C\frac{dv_C}{dt} = i_L - i_o \approx i_L \tag{12}$$

Averaging over one switching period gives:

$$\frac{di_L}{dt} = \frac{1}{L}(v_s - (1-d)v_C) \tag{13}$$

$$\frac{dv_C}{dt} = \frac{1}{C}((1-d)i_L) \tag{14}$$

Since the inductor current remains unaffected

$$i_L(t) \approx I_L \approx \text{constant} \tag{15}$$

Then the dynamics reduce to a single first-order charging law:

$$\frac{dv_C}{dt} = \frac{(1-d)I_L}{C} \tag{16}$$

If $d \approx D$ during this short interval:

$$v_C(t) = V_0 + \frac{(1-D)I_L}{C}t \tag{17}$$

$v_C(t)$ rises linearly until it reaches V_{th}.

$$t_{ch} = \frac{C(V_{th} - V_0)}{(1-D)I_L} \tag{18}$$

where t_{ch} is the charging time.

Mode II: Charging the Capacitor with the Inactive Switch

In this mode, the switch is deactivated, thereby interrupting its role in sustaining the inductor current. As a result, the inductor current gradually decreases but continues to charge the capacitor through the diode. The equivalent circuit for this mode is shown in Fig. 10.

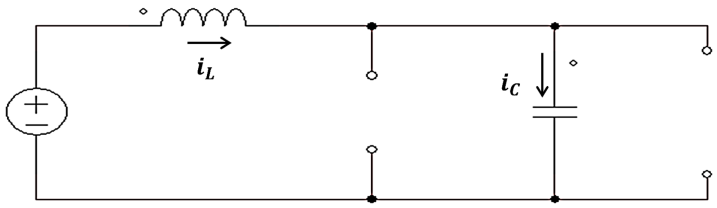


Figure 10: Equivalent circuit for mode II

In this situation, the inductor current can only flow into the capacitor; therefore, the capacitor current is equal to the inductor current. Since the capacitor voltage has already reached the threshold, the inductor current continues to increase the capacitor voltage. The system model in this mode can be expressed as follows:

Let the moment the controller shuts off the gate be $t = 0$:

The initial conditions are: $v_C(0) = V_{th}, i_L(0) = I_L$.

With switch OFF and diode ON:

$$L\frac{di_L}{dt} = v_s - v_C \tag{19}$$

$$C\frac{dv_C}{dt} = i_L \tag{20}$$

From Eq. (19), the discharging time t_{dis} can be calculated as:

$$L\frac{di_L}{dt} = -(V_{th} - V_s) \tag{21}$$

Integrating both sides, the inductor current is:

$$i_L(t) = I_L - \frac{(V_{th} - V_s)}{L}t \tag{22}$$

At t_{dis}, $i_L(t_{dis}) = 0$:

$$0 = I_L - \frac{(V_{\text{th}} - V_s)}{L} t_{dis} \tag{23}$$

$$t_{dis} = \frac{LI_L}{V_{\text{th}} - V_s} \tag{24}$$

From Eq. (20), the maximum value of the capacitor voltage can be expressed as:

$$\frac{dv_C}{dt} = \frac{1}{C}\left(I_L - \frac{(V_{\text{th}} - V_s)}{L} t\right) \tag{25}$$

Integrate with $v_C(0) = V_{\text{th}}$:

$$v_C(t) = V_{\text{th}} + \frac{I_L}{C} t - \frac{(V_{\text{th}} - V_s)}{2LC} t^2 \tag{26}$$

the capacitor voltage reaches its maximum $V_{\max}$ at t_{dis}:

$$V_{\max} = v_C(t_{dis}) \tag{27}$$

Substitute $t_{dis} = \dfrac{LI_L}{V_{\text{th}} - V_s}$:

$$V_{\max} = V_{\text{th}} + \frac{LI_L^2}{2C(V_{\text{th}} - v_s)} \tag{28}$$

Mode III: Relaxed System

Finally, once the inductor is completely discharged, the diode becomes reverse-biased, and the capacitor is fully charged to a voltage slightly above the reference value. The equivalent circuit for this mode is presented in Fig. 11.

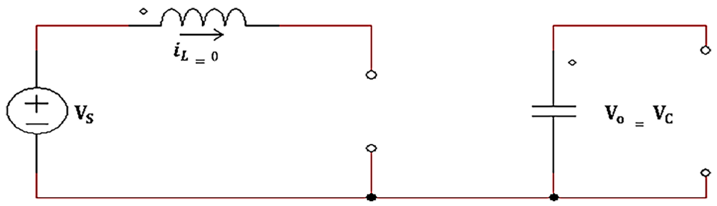


Figure 11: Equivalent circuit for mode III

Fig. 12 illustrates the converter behaviour following load disconnection in three sequential modes governed by energy transfer. In Mode I, immediately after the load is removed, the MOSFET switch continues to receive PWM pulses, so the inductor current remains approximately at its regulated value due to current continuity. Since the load current becomes zero, the capacitor cannot discharge, and the average capacitor current becomes positive, equal to the inductor current during the diode conduction interval. Consequently, the capacitor voltage increases gradually (approximately linearly) until it reaches the predefined threshold. At this instant, the controller disables the gate signal, initiating Mode II. In Mode II, although the switch is turned off, the inductor still stores magnetic energy and continues to discharge through the diode into the capacitor. The inductor current decays approximately linearly because it now experiences a nearly constant negative voltage, while the capacitor voltage increases in a quadratic manner due to the decreasing charging current. This mode ends when the inductor current reaches zero. In Mode III, the inductor is fully discharged, the diode ceases conduction, and

no further current flows; therefore, the capacitor remains charged at its maximum value, slightly above the threshold, determined by the residual energy initially stored in the inductor.

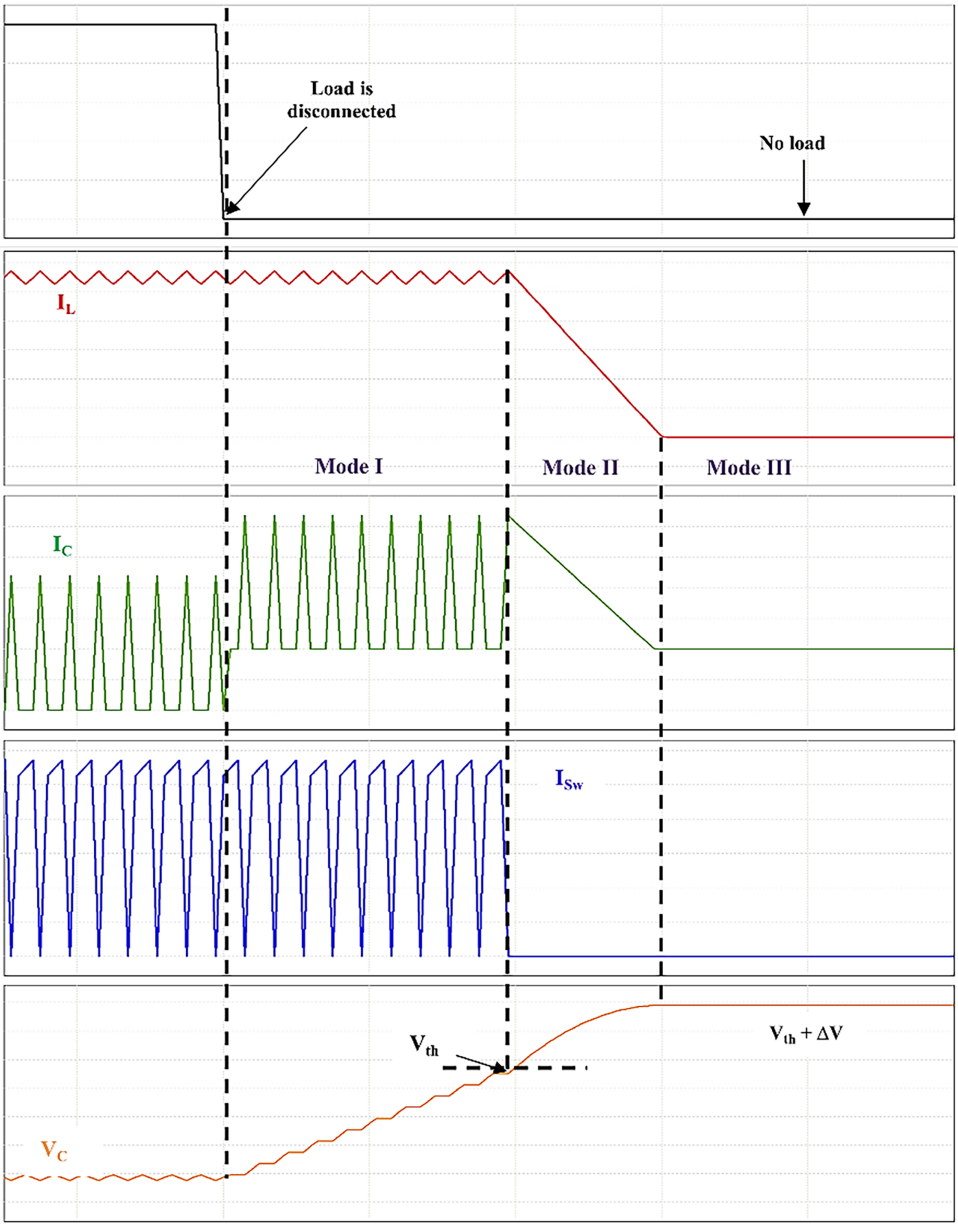


Figure 12: Inductor current waveform (red), capacitor current waveform (green), MOSFET current waveform (blue) and capacitor voltage waveform (orange)

3 Methodology

The proposed control circuit is illustrated in Fig. 13 and operates as follows. In the voltage control loop, a reference voltage is assigned and compared with the measured output voltage. The resulting error signal is scaled by a proportional gain and then limited using a saturation block. The output of

the limiter is subsequently compared with a sawtooth waveform, and the result is applied to one input of an AND gate. Meanwhile, current control is achieved by comparing the sensed input (or inductor) current with a predefined reference to restrict its value. The output of this comparator is fed to the other input of the AND gate. Finally, the AND gate output generates the PWM signal required to drive the converter switch.

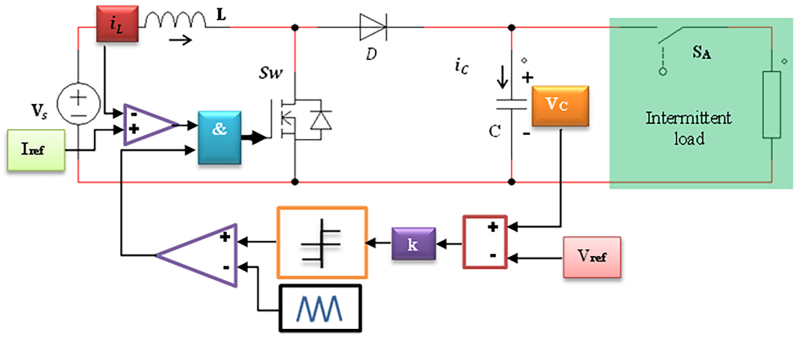


Figure 13: Proposed control circuit implemented to a DC-DC boost converter

The converter parameters are selected based on the equations given below:

$$L = \frac{D(1-D)^2 R}{2f} \tag{29}$$

$$C = \frac{I_o D}{f \Delta V_o} \tag{30}$$

For a duty cycle of $D = 0.3$, the inductance is selected based on the average requirement across the full-load to no-load operating range to ensure stable performance. The capacitance is chosen to keep the DC-link voltage deviation within the minimum acceptable limits. In addition, various capacitor values are tested to evaluate their stiffness and assess their impact on voltage stability and dynamic performance.

4 Simulation

This section presents the simulation results used to evaluate the performance and effectiveness of the proposed control technique, implemented in PLECS software. The control method is applied to a boost converter operating under an intermittent load, where the load switch is periodically turned on and off with different duty cycles for various capacitor values (500, 1000, and 2200 μF). The converter parameters are summarised in Table 1.

Table 1: Boost converter parameters

#	Parameter	Value
1	Input voltage (V_S)	72 V
2	Reference voltage (V_{ref})	100 V
3	Inductor (L)	50 μH

(Continued)

Table 1 (continued)

#	Parameter	Value
4	Capacitor (C)	500, 1000, 2200 μF
5	Full load current (I_o)	10 A
6	Reference current (I_{ref})	14 A
7	Gain constant (k)	10
8	Switching frequency (f_{sw})	10 kHz
9	Load switching frequency (f)	50 Hz

5 Results Analysis

Fig. 14 indicates the capacitor voltage fluctuations when C = 500 μF under the conditions. When the load is disconnected, the voltage jumps to 100.465 V, which is above the reference (100 V) by 0.465 V approximately. However, when a load of 10 A is connected to the converter, the voltage drops to a value that is confined between 99.7 and 100 V (fluctuates between these values). While Fig. 15 indicates the performance of the converter under intermittent load with case 5 A (half-load current). In this case, when the load is disconnected, the voltage jumps to 100.365 V, which is above the reference (100 V) by 0.365 V approximately. However, when a load of 5 A is connected to the converter, the voltage drops to a value that is confined between 99.8 and 100.2 V (fluctuates between these values). It is worth noting that the reference inductor current is maintained at a constant value of 14 A, selected to correspond to a full-load current of 10 A (assuming $P_i = P_o$). As illustrated in the figures, when the load current decreases, the output-voltage fluctuations increase, and the average voltage shifts upward. This widening of the voltage fluctuation band occurs because the converter enters discontinuous conduction mode at light-load conditions. To mitigate this issue, the reference inductor current can be updated according to the power balance relationship to maintain a consistent transformation ratio. The reference input current can be calculated from the power balance equation as

$$I_{ref} = \frac{V_o I_o}{V_s} \tag{31}$$

However, it should be noted that as long as the voltage fluctuation band remains within the predefined acceptable limit, the system performance is not significantly affected, and no adaptive correction is required. Furthermore, the voltage jump between loaded and no-load conditions can be reduced by employing larger output capacitors. Table 2 presents the voltage jumps for various capacitor values. It is evident that a capacitor of 500 μF results in only a slight change, approximately 0.3 V, between half-load and full-load conditions, while values of 1000 μF or higher yield nearly identical voltage jumps across the same load range. This indicates that achieving a constant and robust voltage level in an MLI, independent of load variations, requires careful selection or optimization of the capacitor value.

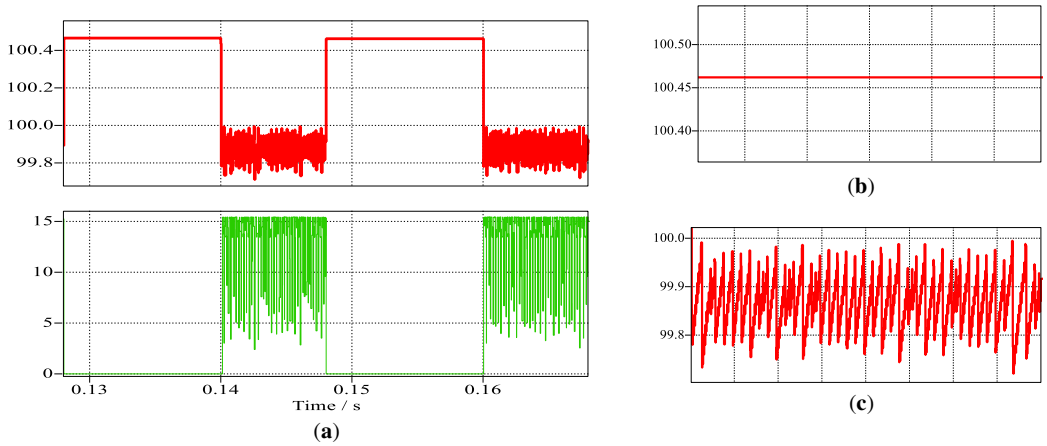


Figure 14: (a) Capacitor voltage (red) and inductor current (green) waveforms for intermittent load, (b) voltage at no-load condition, (c) voltage ripples at full-load condition

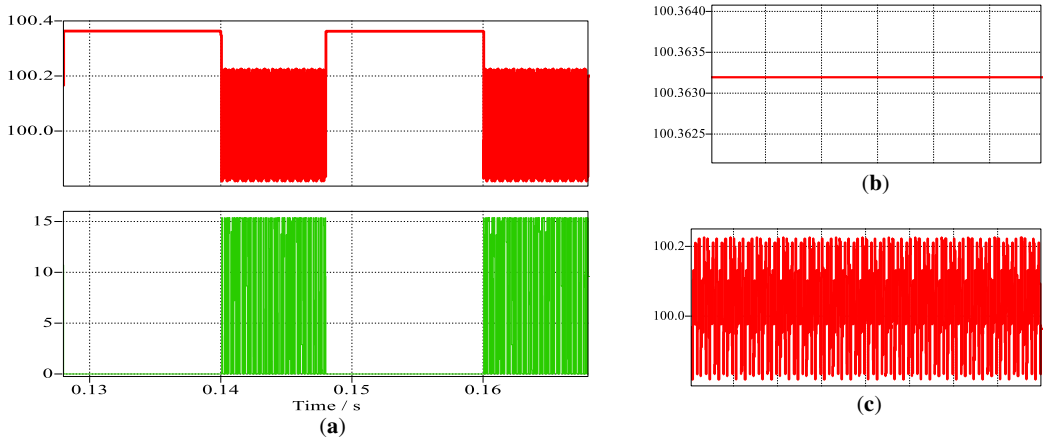


Figure 15: (a) Capacitor voltage (red) and inductor current (green) waveforms for intermittent load, (b) voltage at no-load condition, (c) voltage ripples at half-load condition

Table 2: Voltage jumps for various capacitor values

Capacitor value (μF)	Voltage transition from full and half loads to no-load condition (V)	
	At 5 A	At 10 A
500	0.55	0.8
1000	0.4	0.4
2200	0.2	0.2

5.1 Comparative Analysis

Fig. 16 illustrates the performance comparison of the proposed CVCC controller with the proportional-integral (PI), fuzzy logic (FL), and sliding mode control (SMC) controllers. At t = 0.2 s, the load is disconnected. As observed, the outputs of the PI and FL controllers (red and blue) exhibit instability and gradually diverge. The SMC responds with a voltage jump to 31 V, corresponding to a 3.33% deviation, and subsequently maintains this value. Although the SMC demonstrates improved stability relative to the PI and FL controllers, its design complexity is significantly higher. In contrast, the proposed CVCC controller exhibits superior robustness and stability, with the output voltage increasing only to 30.15 V, corresponding to a 0.5% deviation. Table 3 presents a comparative analysis of the PI, FL, SMC, and CVCC controllers.

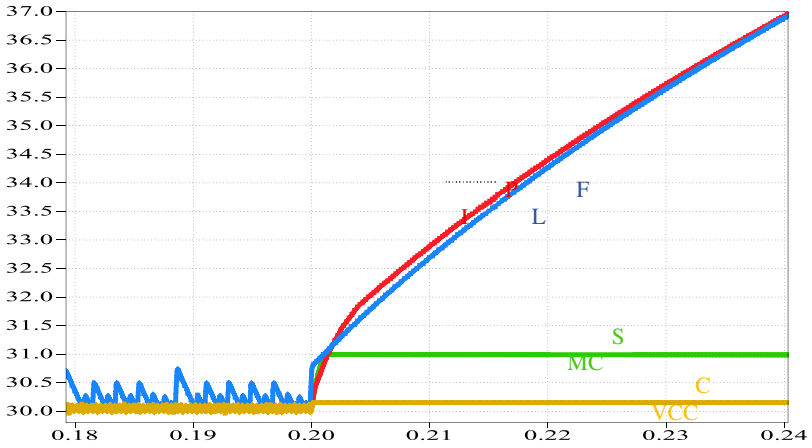


Figure 16: Comparison between the existing control methods and the proposed CVCC

Table 3: Comparison between the PI, FL, SMC, and CVCC controllers under intermittent load

Feature	PI	FL	SMC	CVCC
Control principle	Linear control using proportional + integral action	Rule-based nonlinear control mimicking human reasoning	Nonlinear control with switching surface	Dual-loop control maintains both voltage and current limits
Complexity	Low	Medium	High	Medium
Design effort	Easy tuning (Kp, Ki)	Requires membership functions & rule design	Requires designing a sliding surface & reaching law	Requires designing two loops and reference transitions

(Continued)

Table 3 (continued)

Feature	PI	FL	SMC	CVCC
Robustness to load disturbances	Low; may overshoot or oscillate	Good	Excellent; inherently robust	High
Robustness to parameter variations	Low	Moderate	Very high	High
Stability under intermittent loads	Low	Low	High	Very high
Settling time	–	–	1.2 ms	5 μs
Steady-state error	–	–	3.33%	0.5%

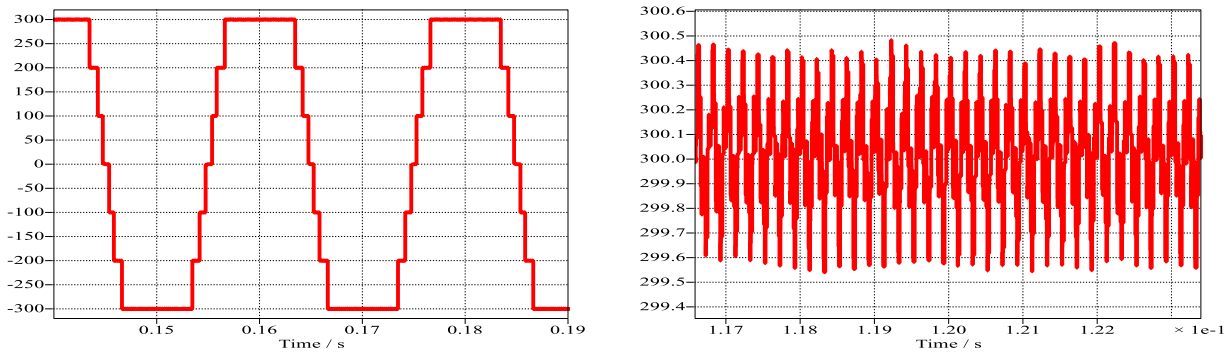
Note: – undefined parameters because the system is unstable.

The Sliding Mode Controller (SMC) exhibits a settling time of 1.2 ms, which reflects its fast dynamic response resulting from the high-gain switching action and the strong corrective behaviour enforced by the sliding surface. Although SMC is well known for its robustness against disturbances and parameter variations, its steady-state error of 3.33% indicates a residual tracking inaccuracy. This error is mainly attributed to practical limitations such as boundary layers introduced to mitigate chattering, which slightly relax the ideal sliding condition and hence reduce steady-state precision.

In contrast, the CVCC strategy demonstrates a remarkably faster settling time of only 5 μs, indicating an almost instantaneous transient response. This superior performance is achieved through its dual-loop structure, which tightly regulates voltage while actively constraining current, allowing rapid corrective action without excessive overshoot. Furthermore, CVCC achieves a very low steady-state error of 0.5%, highlighting its excellent regulation accuracy. The coordinated voltage–current control ensures smooth reference transitions and effective error suppression even under challenging operating conditions such as intermittent or light loads.

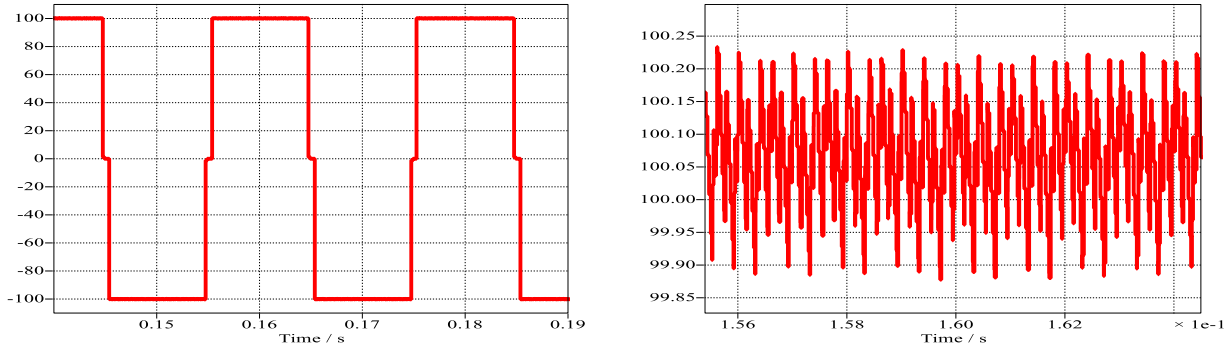
5.2 Implementation to a Multilevel Inverter

To further validate the effectiveness of the proposed method, it was applied to both a single-phase seven-level and a three-level inverter. The simulation results confirm stable and accurate performance under various operating conditions. The multilevel inverter was specifically tested under a light-load condition of 2 A. Fig. 17 shows the seven-level output voltage waveform, where each level is generated by an independent DC-DC boost converter. The results clearly indicate that all voltage levels remain stable, demonstrating the reliability of the proposed method under light-load conditions and confirming its suitability for MLI applications. The voltage ripple at the highest level (300 V) is less than 1 V, corresponding to approximately 0.33%. For real-time validation, the proposed technique was also used to generate a three-level voltage waveform. For comparison, Fig. 18 presents the simulated three-level output, where the maximum voltage is 100 V and the associated ripple is approximately 0.3 V.



(a) (b)

Figure 17: (a) 7-levels voltage waveform (b) voltage ripples



(a) (b)

Figure 18: (a) 3-levels voltage waveform (b) voltage ripples

5.3 Real-Time Validation

In this section, the real-time performance of the proposed control method is evaluated using the PLECS RT Box platform. The objective of this implementation is to validate the effectiveness and practicality of the proposed method under real-time operating conditions. A hardware-in-the-loop (HIL) simulation setup is developed, in which the power circuit model is executed in real time on the PLECS RT Box, while the control algorithm is implemented on an external digital controller. The RT Box and controllers are interconnected through analogue and digital interfaces to enable closed-loop operation. The overall experimental setup used for the HIL simulation is illustrated in Fig. 19.

5.4 DC-DC Boost Converter under Intermittent Load

Fig. 20 shows the capacitor voltage ripples and inductor current of the DC–DC boost converter operating under CVCC control, with the output capacitor set to 500 μF. As illustrated, the output voltage deviation from full load to no load is approximately 0.5 V, corresponding to 0.5% of the nominal output voltage, and occurs at the instant the load is disconnected.

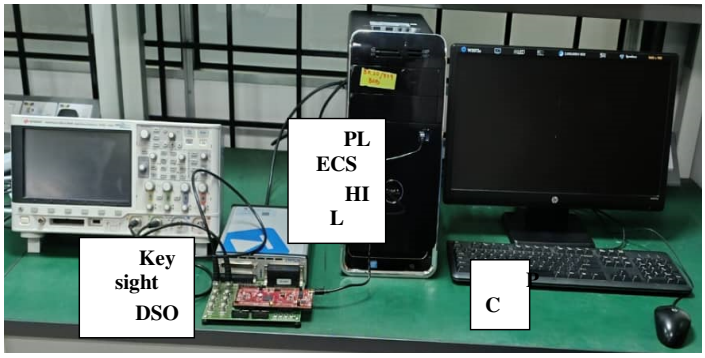


Figure 19: HIL setup

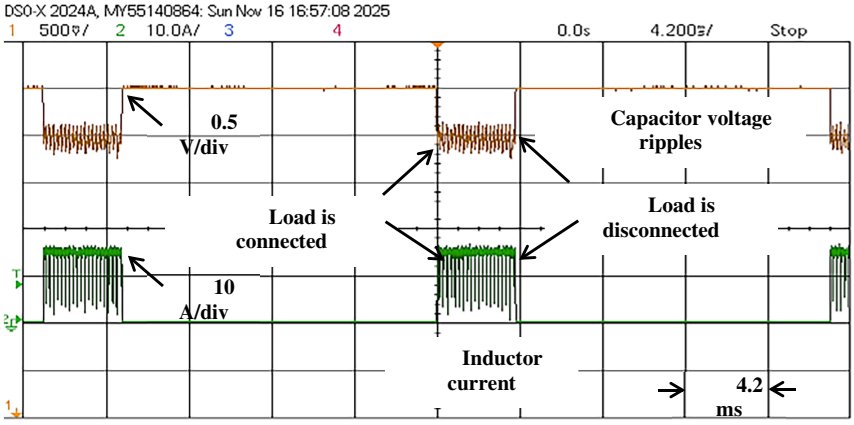


Figure 20: Capacitor voltage ripples and inductor current under intermittent load conditions. Time scale: 4.2 ms/div, Voltage scale: 0.5 V/div, Current scale: 10 A/div

5.5 Implementation of CVCC to Seven-Level and Three-Level Inverters

Figs. 21 and 22 illustrate the output voltage waveforms of the seven-level and three-level inverters operating under the proposed CVCC control strategy. In both cases, at a specific instant, a designated switch is intentionally turned off, thereby disconnecting the load and leaving the corresponding source unloaded. Despite this abrupt change in operating conditions, the output voltage levels remain stable and well-regulated. This result confirms that the CVCC method effectively maintains capacitor voltage balance and mitigates transient disturbances, ensuring reliable and robust inverter performance even during sudden load disconnection events.

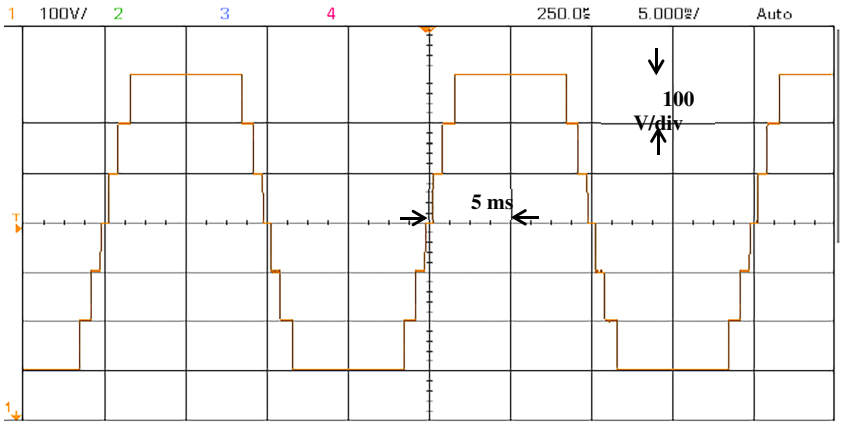


Figure 21: Voltage waveform of a three-level inverter Time scale: 5 ms/div, Voltage scale: 100 V/div

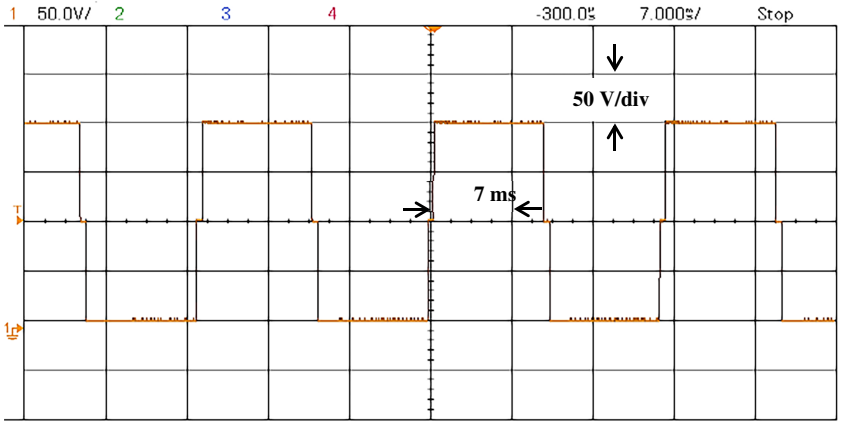


Figure 22: Voltage waveform of a three-level inverter Time scale: 7 ms/div, Voltage scale: 50 V/div

6 Discussion

From the simulation results, it is evident that the converters maintain stable operation even under no-load conditions, i.e., when the inverter switches are disconnected. The accuracy of the voltage levels is further demonstrated by the fact that voltage fluctuations remain below 1 V in the worst case, with a capacitor value of 500 µF and a load current of 10 A. It is also observed that as the load current increases, the average capacitor voltage slightly decreases below the reference value, while increasing the capacitance reduces these fluctuations, thereby enhancing voltage stability. Moreover, with respect to the nominal DC-link voltage of 300 V, the observed deviation of less than 1 V corresponds to only 0.33%, which is significantly lower than the commonly accepted tolerance of ±5% (±15 V) for multilevel inverter systems. This minimal deviation confirms excellent voltage regulation, ensures balanced capacitor voltages, reduces the risk of output distortion, and validates the effectiveness of the proposed method in maintaining reliable inverter operation.

7 Conclusion

This work has presented a direct voltage and current feedback control method for DC–DC converters supplying multilevel inverters. Unlike conventional linear and nonlinear control techniques that often suffer from instability and poor performance under light-load or no-load conditions, the proposed method ensures robust operation by directly regulating both the inductor current and capacitor voltage. Simulation studies conducted in PLECS demonstrated that the converters maintain stable performance even during intermittent load conditions and complete load disconnection. The results further show that the voltage fluctuations at full load, with a 500-μF capacitor, remain minimal, with deviations of less than 1 V, corresponding to only 0.33% of the nominal 300-V DC-link voltage, which is significantly lower than the commonly accepted $\pm$5% tolerance. The proposed method was also validated on single-phase seven-level and three-level inverters, where it achieved accurate voltage regulation, balanced capacitor voltages, and reliable operation under varying load scenarios. For further validation, the system was implemented in a real-time environment and applied to both seven-level and three-level inverters. These findings confirm the effectiveness, stability, and accuracy of the control strategy, highlighting its potential for enhancing the performance and reliability of advanced multilevel power conversion systems.

Acknowledgement: Not applicable.

Funding Statement: This research work supported by Universiti Kebangsaan Malaysia Grant under KK-2023-009 and DPK-2023-015.

Author Contributions: The authors confirm contribution to the paper as follows: Conceptualization, Ahmed Ali and Muhammad Ammirrul Atiqi Mohd Zainuri; methodology, Ahmed Ali; software, Ahmed Ali, Samir Salem Al-Bawri; validation, Praveen Kumar Balachandran, Ahmad Asrul Ibrahim and Muhammad Ammirrul Atiqi Mohd Zainuri; formal analysis, Ahmed Ali and Samir Salem Al-Bawri; investigation, Praveen Kumar Balachandran and Samir Salem Al-Bawri; resources, Ahmed Ali; data curation, Ahmed Ali; writing original draft preparation, Ahmed Ali; writing review and editing, Muhammad Ammirrul Atiqi Mohd Zainuri, Mohd Amran Mohd Radzi and Ahmad Asrul Ibrahim; visualization, Ahmed Ali; supervision, Muhammad Ammirrul Atiqi Mohd Zainuri, Mohd Amran Mohd Radzi and Ahmad Asrul Ibrahim; project administration, Muhammad Ammirrul Atiqi Mohd Zainuri and Mohd Amran Mohd Radzi; funding acquisition, Muhammad Ammirrul Atiqi Mohd Zainuri. All authors reviewed and approved the final version of the manuscript.

Availability of Data and Materials: The data that support the findings of this study are available from the Corresponding Author, [Praveen Kumar Balachandran], upon reasonable request.

Ethics Approval: Not applicable.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Tarzamni H, Gohari HS, Sabahi M, Kyyrä J. Nonisolated high step-up DC-DC converters: comparative review and metrics applicability. IEEE Trans Power Electron. 2024;39(1):582–625. doi:10.1109/tpel.2023.3264172.

2. Arumozhiyal D, Saravanakumar S. Design of fast and zero voltage switching of interleaved flyback converter with H6 type inverter for photovoltaic applications. Revista Internacional de Métodos Numéricos para Cálculo y Diseño en Ingeniería. 2022;38(3):1–11. doi:10.23967/j.rimni.2022.09.006.
3. Balachandran P, Kalpana G, Babyshalini V, Srilakshmi K, Singh S. Optimization of EV and green source fed five-level UPQC for power quality and energy management using fennec fox algorithm. Revista Internacional de Métodos Numéricos para Cálculo y Diseño en Ingeniería. 2025;41(3):44. doi:10.23967/j.rimni.2025.10.66625.
4. Mumtaz F, Zaihar Yahaya N, Tanzim Meraj S, Singh B, Kannan R, Ibrahim O. Review on non-isolated DC-DC converters and their control techniques for renewable energy applications. Ain Shams Eng J. 2021;12(4):3747–63. doi:10.1016/j.asej.2021.03.022.
5. Alkhaldi A, Elkhateb A, Laverty D. Voltage lifting techniques for non-isolated DC/DC converters. Electronics. 2023;12(3):718. doi:10.3390/electronics12030718.
6. Ghamari SM, Hajihosseini M, Habibi D, Aziz A. Design of an adaptive robust PI controller for DC/DC boost converter using reinforcement-learning technique and snake optimization algorithm. IEEE Access. 2024;12:141814–29. doi:10.1109/access.2024.3440580.
7. Seo SW, Choi HH. Digital implementation of fractional order PID-type controller for boost DC-DC converter. IEEE Access. 2019;7:142652–62. doi:10.1109/access.2019.2945065.
8. Mohamed AT, Mahmoud MF, Swief RA, Said LA, Radwan AG. Optimal fractional-order PI with DC-DC converter and PV system. Ain Shams Eng J. 2021;12(2):1895–906. doi:10.1016/j.asej.2021.01.005.
9. Haque MR, Salam KMA, Razzak MA. A modified PI-controller based high current density DC-DC converter for EV charging applications. IEEE Access. 2023;11:27246–66. doi:10.1109/access.2023.3258181.
10. Thaliyadath D, Kaliyaperumal D, Kolhe ML. Enhancing transient response in a DC-DC converter for electric vehicle DC fast charging applications using fractional-order PI control. Energies. 2024;17(17):4312. doi:10.3390/en17174312.
11. Elkeiy MA, Abdelaziz YN, Hamad MS, Abdel-Khalik AS, Abdelrahem M. Multiport DC-DC converter with differential power processing for fast EV charging stations. Sustainability. 2023;15(4):3026. doi:10.3390/su15043026.
12. Zhou S, Zhou G, He M, Mao S, Zhao H, Liu G. Stability effect of different modulation parameters in voltage-mode PWM control for CCM switching DC-DC converter. IEEE Trans Transp Electrif. 2024;10(2):2408–22. doi:10.1109/tte.2023.3293811.
13. Chilukuri GR, Majumder P, Kapat S. Closed-loop stability analysis of digitally current mode controlled three-level buck converter using a simplified discrete-time modeling framework. In: Proceedings of the 2023 IEEE Applied Power Electronics Conference and Exposition (APEC); 2023 Mar 19–23; Orlando, FL, USA. p. 1200–6. doi:10.1109/apec43580.2023.10131217.
14. Geng X, Xu J, Wang L, Chen Z, Huang R. Performance analysis and improvement of PI-type current controller in digital average current mode controlled three-phase six-switch boost PFC rectifier. IEEE Trans Power Electron. 2022;37(7):7871–82. doi:10.1109/tpel.2022.3150068.
15. Buso S, Mattavelli P. Digital current mode control. In: Digital control in power electronics. Cham, Switwerland: Springer International Publishing; 2006. p. 33–79. doi:10.1007/978-3-031-02495-5_3.
16. Hallworth M, Ali Shirsavar S. Microcontroller-based peak current mode control using digital slope compensation. IEEE Trans Power Electron. 2012;27(7):3340–51. doi:10.1109/tpel.2011.2182210.
17. Abdelhamid E, Corradini L, Mattavelli P, Bonanno G, Agostinelli M. Sensorless stabilization technique for peak current mode controlled three-level flying-capacitor converters. IEEE Trans Power Electron. 2020;35(3):3208–20. doi:10.1109/tpel.2019.2930011.
18. Muñoz JG, Gallo G, Angulo F, Osorio G. Slope compensation design for a peak current-mode controlled boost-flyback converter. Energies. 2018;11(11):3000. doi:10.3390/en11113000.
19. Kazimierczuk M, Ayachit A, Saini D. Average current-mode control of DC-DC power converters. Hoboken, NJ, USA: John Wiley & Sons; 2022. doi:10.1002/9781119525592.

20. Patra S, Singha AK. An event-driven sampling mechanism for digital average current-mode controlled boost converter. IEEE Trans Circuits Syst II. 2024;71(3):1456–60. doi:10.1109/tcsii.2023.3321890.
21. Arunkumar G, Dhanamjayulu C, Padmanaban S, Prusty BR, Khan B. Implementation of optimization-based PI controller tuning for non-ideal differential boost inverter. IEEE Access. 2021;9:58677–88. doi:10.1109/access.2021.3071538.
22. Chander S, Agarwal P, Gupta I. Auto-tuned, discrete PID controller for DC-DC converter for fast transient response. In: Proceedings of the India International Conference on Power Electronics 2010 (IICPE2010); 2011 Jan 28–30; New Delhi, India. p. 1–7. doi:10.1109/iicpe.2011.5728120.
23. Ibrahim O, Yahaya NZ, Saad N. Comparative studies of PID controller tuning methods on a DC-DC boost converter. In: Proceedings of the 2016 6th International Conference on Intelligent and Advanced Systems (ICIAS); 2016 Aug 15–17; Kuala Lumpur, Malaysia. p. 1–5. doi:10.1109/icias.2016.7824044.
24. Anto EK, Asumadu JA, Okyere PY. PID control for improving P&O-MPPT performance of a grid-connected solar PV system with Ziegler-Nichols tuning method. In: Proceedings of the 2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA); 2016 Jun 5–7; Hefei, China. p. 1847–52. doi:10.1109/iciea.2016.7603888.
25. da S. C. Pereira LF, Batista E, de Brito MAG, Godoy RB. A robustness analysis of a fuzzy fractional order PID controller based on genetic algorithm for a DC-DC boost converter. Electronics. 2022;11(12):1894. doi:10.3390/electronics11121894.
26. Badis A, Mansouri MN, Boujmil MH. A genetic algorithm optimized MPPT controller for a PV system with DC-DC boost converter. In: Proceedings of the 2017 International Conference on Engineering & MIS (ICEMIS); 2017 May 8–10; Monastir, Tunisia. p. 1–6. doi:10.1109/icemis.2017.8273010.
27. Inomoto RS, de Almeida Monteiro JRB, Filho AJS. Boost converter control of PV system using sliding mode control with integrative sliding surface. IEEE J Emerg Sel Topics Power Electron. 2022;10(5): 5522–30. doi:10.1109/jestpe.2022.3158247.
28. Balta G, Altin N, Nasiri A. Interval type-2 fuzzy-logic-based constant switching frequency control of a sliding-mode-controlled DC-DC boost converter. Appl Sci. 2023;13(5):3239. doi:10.3390/app13053239.
29. Akter F, Roy TK, Islam MS, Alkhateeb AF, Mollah MA. Design of a nonlinear integral terminal sliding mode controller for a PEM fuel cell based on a DC-DC boost converter. IEEE Access. 2022;10:97419–28. doi:10.1109/access.2022.3205733.
30. Malge SV, Ghogare MG, Patil SL, Deshpande AS, Pandey SK. Chatter-free non-singular fast terminal sliding mode control of interleaved boost converter. IEEE Trans Circuits Syst II. 2023;70(1):186–90. doi:10.1109/tcsii.2022.3201959.
31. Kapat S. Chattering-free event-trigger fast recovery stable digital sliding mode control in DC-DC converters. In: Proceedings of the 2022 IEEE Applied Power Electronics Conference and Exposition (APEC); 2022 Mar 20–24; Houston, TX, USA. p. 1248–52. doi:10.1109/apec43599.2022.9773578.
32. Ali M, Yu H, Wang Y, Yang Y. Control of linear generator based on hysteresis-SVPWM current rectification and bidirectional buck/boost converter used for energy storage. IET Renew Power Gener. 2021;15(14): 3282–95. doi:10.1049/rpg2.12251.
33. Muñoz JG, Angulo F, Angulo-Garcia D. Designing a hysteresis band in a boost flyback converter. Mech Syst Signal Process. 2021;147(2):107080. doi:10.1016/j.ymssp.2020.107080.
34. Nethaji G, Kathirvelan J. Performance comparison between PID and Fuzzy logic controllers for the hardware implementation of traditional high voltage DC-DC boost converter. Heliyon. 2024;10(17):e36750. doi:10.1016/j.heliyon.2024.e36750.
35. Rajavel A, Rathina Prabha N. Fuzzy logic controller-based boost and buck-boost converter for maximum power point tracking in solar system. Trans Inst Meas Control. 2021;43(4):945–57. doi:10.1177/0142331220938211.

36. Dong W, Li S, Fu X, Li Z, Fairbank M, Gao Y. Control of a buck DC/DC converter using approximate dynamic programming and artificial neural networks. IEEE Trans Circuits Syst I. 2021;68(4):1760–8. doi:10.1109/tcsi.2021.3053468.
37. Srinivasan S, Tiwari R, Krishnamoorthy M, Lalitha MP, Raj KK. Neural network based MPPT control with reconfigured quadratic boost converter for fuel cell application. Int J Hydrogen Energy. 2021;46(9):6709–19. doi:10.1016/j.ijhydene.2020.11.121.
38. Marahatta A, Rajbhandari Y, Shrestha A, Phuyal S, Thapa A, Korba P. Model predictive control of DC/DC boost converter with reinforcement learning. Heliyon. 2022;8(11):e11416. doi:10.1016/j.heliyon.2022.e11416.
39. Wang D, Shen ZJ, Yin X, Tang S, Liu X, Zhang C, et al. Model predictive control using artificial neural network for power converters. IEEE Trans Ind Electron. 2022;69(4):3689–99. doi:10.1109/tie.2021.3076721.
40. Viswambharan A, Errouissi R, Debouza M, Shareef H. Experimental verification of disturbance observer-based backstepping control for DC-DC boost converter. IEEE Trans Circuits Syst I. 2023;70(12):5520–33. doi:10.1109/tcsi.2023.3318970.
41. Hassan M, Su CL, Chen FZ, Lo KY. Adaptive passivity-based control of a DC–DC boost power converter supplying constant power and constant voltage loads. IEEE Trans Ind Electron. 2022;69(6):6204–14. doi:10.1109/tie.2021.3086723.
42. Reverter F, Gasulla M. Optimal inductor current in boost DC/DC converters operating in burst mode under light-load conditions. IEEE Trans Power Electron. 2016;31(1):15–20. doi:10.1109/tpel.2015.2454331.
43. Suntio T. Modeling and analysis of a PCM-controlled boost converter designed to operate in DCM. Energies. 2019;12(1):4. doi:10.3390/en12010004.
44. Kapat S, Mandi BC, Patra A. Voltage-mode digital pulse skipping control of a DC–DC converter with stable periodic behavior and improved light-load efficiency. IEEE Trans Power Electron. 2016;31(4): 3372–9. doi:10.1109/tpel.2015.2455553.
45. Magdy M, Hanafy F, Abou-Zalam B, Nabil E. Optimized Multi-Stepped constant current constant voltage fast charging controller for lithium-ion batteries. Sci Rep. 2025;15(1):40359. doi:10.1038/s41598-025-25924-2.
46. Zhang Y, Shen Z, Pan W, Wang H, Wu Y, Mao X. Constant current and constant voltage charging of wireless power transfer system based on three-coil structure. IEEE Trans Ind Electron. 2023;70(1):1066–70. doi:10.1109/tie.2022.3150112.