Design and Performance of an Ultra Gain Boost Converter for Solar-Powered Electric Vehicle Applications

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INFORMATION

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ABSTRACT

This paper presents the design and performance analysis of an Ultra Gain Boost Converter (UGBC) intended for solar-powered electric vehicle (SPEV) applications. The proposed converter is derived from a cascaded boost–boost structure with a capacitor–diode voltage-lift cell, allowing high voltage gain without operating at extreme duty ratios. The proposed structure provides continuous input current, improved voltage boosting capability, and reduced voltage stress on semiconductor devices, making it suitable for photovoltaic based energy systems. Complete steady-state analysis, voltage-gain derivation, device stresses estimation, power-loss estimation, and small-signal dynamic modelling are carried out to evaluate the converter characteristics. The UGBC topology is validated with MATLAB/Simulink simulations for an operating condition of 24 to 72 V at a duty ratio of 0.33, indicating stable voltage regulation, low current ripple, and higher efficiencies. Additionally, system-level performance is given by interfacing the converter with a BLDC motor drive, where stable speed regulation and smooth torque response are observed. The results confirm that the proposed UGBC converter with a capacitor–diode cell is a feasible and efficient solution for high-gain Ultra Gain DC–DC conversion in solar-based electric mobility applications.

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Nomenclature

Symbol	Description
(V_{in})	Input voltage of the UGBC
(V_0)	Output voltage of the UGBC
(I_{in})	Input current
(I_0)	Output current

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(D)	Duty ratio of the active switches
(f_S)	Switching frequency
(L_x, L_y)	Inductors of the cascaded boost stages
(C_x, C_y, C_z)	Capacitors of the voltage-lift and output stages
(S_x, S_y)	Active power switches
(D_x, D_y, D_z)	Diodes in the voltage-lift and output paths
(R)	Load resistance
(G)	Steady-state DC voltage gain
(i_{Lx}, i_{Ly})	Currents through inductors (L_x) and (L_y)
(v_{Cx}, v_{Cy}, v_{Cz})	Voltages across capacitors (C_x, C_y), and (C_z)
CCM	Continuous conduction mode
MPPT	Maximum power point tracking
UGBC	Ultra Gain Boost Converter
SPEV	Solar-powered electric vehicle
BLDC	Brushless DC motor

1 Introduction

The growing emphasis on clean and sustainable transportation has intensified research on solar-powered electric vehicles (SPEVs), where photovoltaic (PV) sources are employed to support or supplement conventional energy storage systems. By enabling partial on-board energy harvesting, SPEVs can reduce dependency on grid-based charging infrastructure and contribute to the reduction of greenhouse-gas emissions. A major technical challenge in SPEVs is the large voltage mismatch between low-voltage PV modules, which typically operate in the range of 12–48 V, and the high-voltage DC links required by electric-vehicle (EV) traction drives and auxiliary systems, which commonly exceed 200–400 V [1]. Addressing this mismatch efficiently requires compact, high step-up DC–DC converters capable of providing large voltage gains with high efficiency and reliable operation. The general energy conversion architecture of a solar-powered electric vehicle, highlighting the role of the high-gain DC–DC converter between the PV source and the electric drive system, is illustrated in Fig. 1.

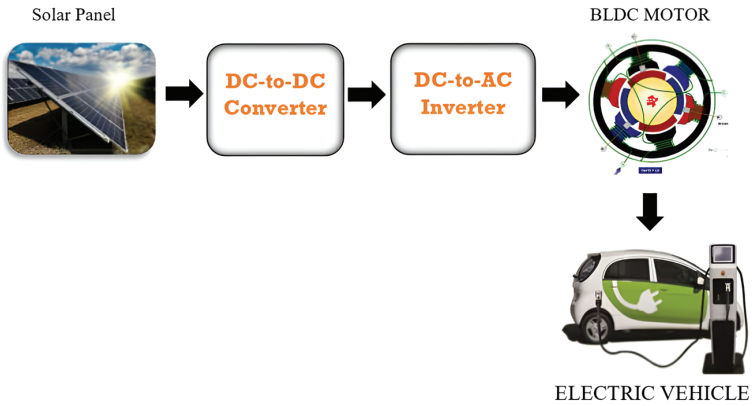


Figure 1: General architecture of a solar-powered electric vehicle with the integration of the photovoltaic source, high-gain DC–DC converter, inverter, and electric drive system

Conventional boost and buck–boost converters are widely adopted because of their simple structure and ease of control. However, their achievable voltage gain is inherently limited, and high step-up conversion can only be achieved by operating at extreme duty ratios. Such operating conditions result in increased conduction and switching losses, severe voltage and current stress on semiconductor devices, and reduced overall efficiency [2]. In addition, buck–boost converters draw discontinuous input current, which is undesirable for PV-fed systems employing maximum power point tracking (MPPT). Isolated converter topologies, such as flyback and forward converters, are capable of higher voltage gain; nevertheless, the use of high-frequency transformers increases system size, cost, and design complexity, making these converters less attractive for compact SPEV applications [3].

In response to these limitations, several non-isolated high-gain DC–DC converter topologies have been reported in the literature, including quadratic boost converters, switched-capacitor converters, switched-inductor structures, and cascaded configurations [4–8]. Quadratic boost converters enhance voltage gain through multistage energy transfer, but this improvement is often accompanied by an increased number of passive components, higher current ripple, and elevated device stress [4,5]. Switched-capacitor converters can achieve large voltage multiplication without magnetic coupling; however, they typically suffer from high peak currents and reduced efficiency when operating at higher power levels [6]. Cascaded boost configurations offer improved gain scalability, yet without appropriate voltage-lift mechanisms they still rely on large duty ratios and impose significant stress on power semiconductor devices [7,8].

Several recent studies have shown that the integration of capacitor–diode voltage-lift cells within non-isolated boost-based architectures can significantly enhance voltage gain while alleviating device stress and maintaining continuous input current [9–12]. Such approaches improve voltage boosting capability without employing magnetic coupling or isolation and are therefore attractive for renewable-energy-based systems. Despite these advances, many reported high-gain converters still suffer from increased circuit complexity, uneven distribution of voltage and current stress, or limited discussion on dynamic performance and practical system-level applicability [13–16]. Moreover, although electric-mobility applications are frequently cited as target use cases, the interaction between high-gain DC–DC converters and electric drive systems is often not explicitly demonstrated.

Motivated by the above observations, this paper proposes an Ultra Gain Boost Converter (UGBC) realized using a cascaded boost–boost structure augmented with a capacitor–diode voltage-lift cell. The proposed UGBC achieves enhanced voltage gain at moderate duty ratios without employing magnetic coupling or isolation, while maintaining continuous input current and reduced voltage stress across power semiconductor devices. A detailed analytical framework is presented, covering steady-state modelling, voltage-gain derivation, component stress analysis, power-loss evaluation, and small-signal dynamic modelling. In addition, the practical suitability of the proposed UGBC is validated through comprehensive simulations and system-level integration with a brushless DC (BLDC) motor drive, demonstrating its relevance for solar-powered electric-vehicle applications [17].

The main contributions of this work can be summarized as follows:

- Development of a cascaded boost–boost UGBC integrating a capacitor–diode voltage-lift cell to achieve high voltage gain with moderate duty ratios.
- Comprehensive analytical modelling of the proposed UGBC, including voltage gain, device stress evaluation, power-loss estimation, and small-signal dynamic analysis.
- Comparative performance assessment of the UGBC against recently reported high-gain DC–DC converters in terms of voltage gain, device stress, and effectiveness index.

- System-level validation of the proposed converter through BLDC motor drive integration, demonstrating stable speed regulation and smooth torque characteristics suitable for electric-mobility applications.

Research Gap and Motivation

Recent studies on non-isolated high step-up DC–DC converters have explored quadratic boost, switched-capacitor, switched-inductor, and cascaded structures to address the voltage mismatch between low-voltage renewable sources and high-voltage DC links [4–8]. Capacitor–diode voltage-lift techniques have also been reported as an effective means of improving voltage gain while reducing device stress [9–12]. Despite these efforts, several challenges remain unresolved for practical solar-powered electric vehicle applications.

Most existing high-gain converters achieve large voltage gain only at high duty ratios or with increased component count, which leads to higher losses, increased current ripple, and reduced efficiency [4,5,13]. In addition, uneven distribution of voltage and current stress among semiconductor devices is still commonly observed, negatively affecting reliability and device utilization [10,14,15]. Furthermore, many studies emphasize steady-state gain enhancement, while dynamic behaviour, small-signal characteristics, and system-level validation with electric drives are often insufficiently addressed [16].

Motivated by these gaps, this work proposes an UGBC based on a cascaded boost–boost structure with a capacitor–diode voltage-lift cell. The objective is to achieve enhanced voltage gain at moderate duty ratios while maintaining continuous input current, reduced device stress, and high efficiency. The proposed UGBC is evaluated through analytical modelling, comparative assessment, and system-level validation with a BLDC motor drive, addressing both converter-level performance and application-oriented requirements relevant to solar-powered electric vehicle systems.

2 Structural Design of the Proposed UGBC

This part explains the circuit topology, working operation, and steady-state analysis of the given Ultra Gain Boost Converter (UGBC). The design is specially developed for realizing a scalable ultra-high voltage gain while reducing voltage and current stress to power semiconductor devices, thus being most suitable for SPEV applications.

2.1 Circuit Topology and Operating Principle

The proposed Ultra Gain Boost Converter (UGBC) is a non-isolated, single-stage DC–DC topology formed by cascading two conventional boost converters and integrating a capacitor–diode voltage-lift cell. The cascaded boost structure enhances the voltage conversion ratio, while the voltage-lift cell further increases the input of the second boost stage without requiring extreme duty-cycle operation. This configuration ensures continuous input current and distributes voltage stress across the semiconductor devices, making the proposed UGBC suitable for photovoltaic-fed electric vehicle applications.

Fig. 2 shows the circuit configuration of the proposed UGBC. Capacitors $\boldsymbol{C}_x$ and $\boldsymbol{C}_y$ are charged in parallel during a single switching phase and discharged in series with the source during the other, multiplying the voltage supplied to inductor $\boldsymbol{L}_y$. This allows the converter to be able to have a high voltage gain without the need for an extreme duty cycle or large turns ratio in a magnetic device.

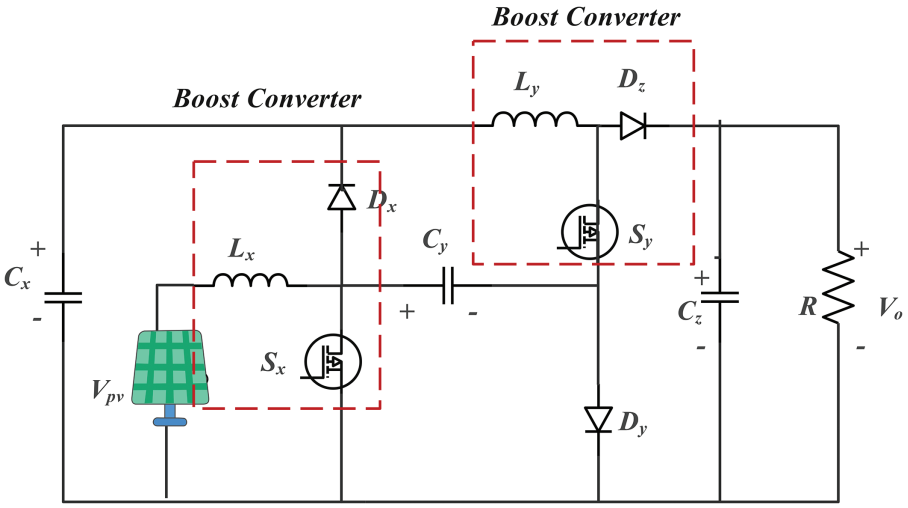


Figure 2: Ultra gain boost converter

2.1.1 Key Benefits

- Continuous Input Current: Supplied by inductor $\boldsymbol{L_x}$ and is compatible with MPPT algorithms for PV sources.
- Less Device Stress: The hybrid topology shares voltage and current stresses among components more evenly than traditional quadratic boost converters.
- Scalable High Gain: The theoretical voltage gain is expressed by $\boldsymbol{M_{ccm} = (1+D)/(1-D)^2}$, which is greater than 10x at realistic duty cycles (e.g., $D = 0.67$ corresponds to $M \approx 15$).

The converter is in Continuous Conduction Mode (CCM) with ideal components and large enough capacitors for maintaining a constant output voltage. Its operation is separated into two distinct modes in a single switching period ($\boldsymbol{T_S}$) shown in Table 1.

Table 1: Operating modes in CCM

Mode	S_x, S_y	D_x, D_y, D_z	L_x, L_y	C_x, C_y, C_z
Mode-1	ON	OFF	Charging	Discharging
Mode-2	OFF	ON	Discharging	Charging

Mode I: Switches ON ($0 < t < DT_S$):

In this period, switches $\boldsymbol{S_x}$ and $\boldsymbol{S_y}$ are turned ON, on the other hand all diodes ($\boldsymbol{D_x}$, $\boldsymbol{D_y}$, $\boldsymbol{D_z}$) are reverse-biased. The corresponding circuit is given in Fig. 3a. In this state, the input voltage directly energizes the inductors, resulting in a linear increase in their currents. The diode associated with the capacitor–diode voltage-lift cell is reverse-biased, isolating the capacitor from the load. Consequently, the voltage-lift capacitor is charged. Meanwhile, the output capacitor supplies the load current, maintaining the output voltage. This operating mode allows energy to be stored in the inductors while maintaing continuous input current. The governing equations for Mode I are:

$$\boldsymbol{V_{L_x} = V_{pv}} \tag{1}$$

$$V_{L_y} = V_{C_x} + V_{C_y} \tag{2}$$

$$I_{C_z} = I_y = -I_{L_y}; I_{C_z} = \frac{V_0}{R}; I_{C_z} = -I_0 \tag{3}$$

here, V_{L_x} and V_{L_y} represent the voltages across inductors L_x and L_y, while V_{C_x} and V_{C_y} denote capacitor voltages. Similarly, I_{L_x} and I_{L_y} are the inductor currents, and I_{C_z} is the output capacitor current.

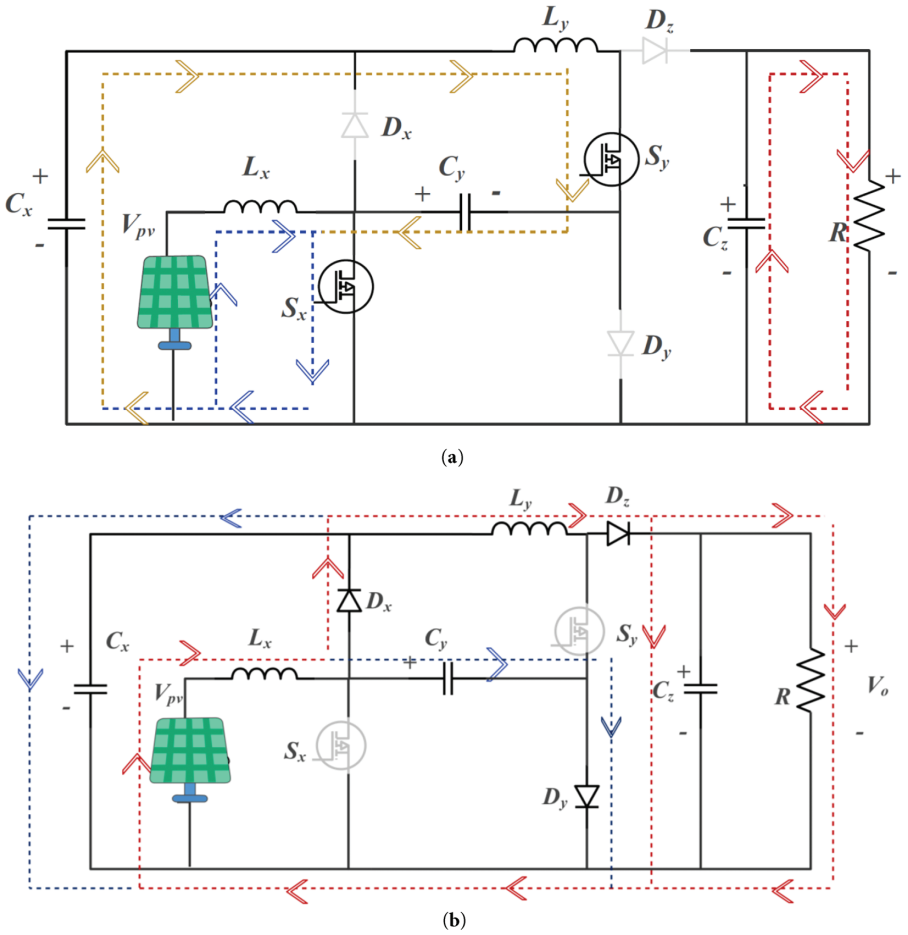


Figure 3: (**a**) Circuit conditions in mode-1. (**b**) Circuit conditions in mode-II

Mode II: Switches OFF ($DT_S < t < T_S$):

In this period, switches S_x and S_y are turned OFF, hence all diodes are forward-biased. The corresponding circuit is given in Fig. 3b. In this state the converter transitions into the energy transfer interval. The stored energy in the inductors is released through the corresponding diodes toward the output stage. During this interval, the voltage stored across the capacitor is effectively added in series with the input and inductor voltages. This combined voltage significantly enhances the effective input of the second boost stage, resulting in an increased output voltage. Simultaneously, the output capacitor is recharged while supplying the load. The governing equations for Mode II are:

$$V_{L_x} = V_{in} - V_{C_x};$$

$$V_{Cx} = V_{in} - V_{Lx};$$
$$V_{Lx} = V_{in} - V_{Cy};$$
$$V_{Cy} = V_{in} - V_{Lx};$$
$$V_{Ly} = V_{Cx} - V_0 \tag{4}$$
$$I_{Cz} = I_{Ly} - I_0 \,(or)\, I_{Cz} = I_{Ly} - \frac{V_0}{R}$$
$$I_{Cx} = I_{Cy} = \frac{I_{Lx} - I_{Ly}}{2} \tag{5}$$

These equations describe the energy transfer mechanism between inductors, capacitors, and the load resistance during the OFF state of the switching cycle. As shown in Fig. 3, the voltage gain of the UBGC topology is determined by the volt-second equilibrium principle. This rule ensures that the total voltage across an inductor over one full switching cycle is zero during steady-state operation.

When the switch is ON, the inductors accumulate energy, and when the switch is OFF, this energy is transferred to the capacitors and the load. By applying this principle to the inductors Lx and Ly, a formula can be derived that connects the output voltage, input voltage, and duty cycle (D) [4]. This formula determines the converter ability to boost the voltage, making a better solution for EVs and other renewable energy applications.

2.1.2 Voltage Gain of the Converter

$$V_{Lx} = 0 = V_{in} \cdot D + (V_{in} - V_{Cx}) \cdot (1 - D)$$
$$V_{Ly} = 0 = (V_{Cx} + V_{Cy}) \cdot D + (V_{Cx} - V_o) \cdot (1 - \mathrm{D}) \tag{6}$$

The steady-state voltage across the capacitors can be expressed, by solving the equations derived from the volt-sec equilibrium principle, as:

$$V_{Cx} = V_{Cy};$$
$$V_{Cy} = \frac{V_{in}}{[1 - D]} \tag{7}$$

Eqs. (6) and (7) are used to find the voltage gain of the projected UGBC network under CCM mode.

The gain formula is:

$$M_{ccm} = \frac{V_0}{V_{in}} = \frac{(1 + D)}{(1 - D)^2} \tag{8}$$

The current gain of the topology is estimated by means of the ampere-second equilibrium law on the capacitor. The ampere-second balance indicates that, within one switching cycle, the net charge transferred to the capacitor must be zero. The ampere-second balance lets us establish the relationship between input and output currents, and thus determine the current gain for the converter. Using Eqs. (3) and (5), the average inductor current and current gain can be expressed as follows:

$$I_{C1} = I_{C1} = 0 = -I_{L2} - \frac{I_{L1} - I_{L2}}{2}(1 - D)$$

$$I_{L_y} = I_o;$$
$$I_{L_y} = \frac{I_0}{(1-d)}; I_{in} = I_{L_x};$$
$$I_{in} = \frac{I_0\,(1+D)}{(1-D)^2} \tag{9}$$
$$M_{ccm_I} = \frac{I_{in}}{I_0} = \frac{(1+D)}{(1-D)^2} \tag{10}$$

The steady-state equations previously derived hold great significance for evaluating various performance characteristics of the converter. In particular, they are useful for assessing the electrical stresses on active switches, selecting the values of the circuit, and estimating overall system efficiency. Understanding these relationships allows engineers to improve operation, reliability, and energy efficiency for the converter. The steady-state analysis and voltage-gain derivation are based on conventional volt–second balance principles widely adopted in high-gain DC–DC converter analysis [4,5,8].

2.2 Electromagnetic Impacts on Power Device Integrity

The voltage and current stress expressions are derived using standard analysis approaches reported in literature [6,9,10]. The voltage and current stresses across the passive components are evaluated under steady-state CCM operation to ensure safe device ratings and reliable converter performance. The voltage stress for each component can be calculated by analyzing the behaviour and the corresponding Eqs. (7)–(10) under steady-state. The detailed expressions will be presented below.

$$V_{S_x} = V_{C_x} = \frac{V_{in}}{1-D}$$
$$V_{S_y} = V_{C_y} = \frac{V_{in}}{1-D} \tag{11}$$

Voltage Stress on Diodes D_x, D_y, and D_z are given by,

$$V_{D_x} = V_{C_x} = \frac{V_{in}}{1-D}$$
$$V_{D_y} = V_{C_y} = \frac{V_{in}}{1-D}$$
$$V_{D_z} = V_0 = \frac{1+D}{(1-D)^2} \times V_{in} \tag{12}$$

Similar to voltage stress, the current stress imposed on a power device is obtained as

$$I_{S_x} = [I_{L_x} + I_{L_y}]D = \frac{2D}{(1-D)^2} \times I_0$$
$$I_{S_y} = I_{L_y}D = \frac{D}{(1-D)} \times I_0$$

$$I_{D_x} = \frac{I_{L_x} + I_{L_y}}{2}(1-D) = \frac{I_0}{(1-D)}$$
$$I_{D_y} = \frac{I_{L_x} - I_{L_y}}{2}(1-D) = \frac{I_0 D}{(1-D)}$$
$$I_{D_z} = I_{L_y}(1-D) = I_0 \tag{13}$$

The RMS current expressions in Eq. (14) for the circuit components can also be used later in calculating the power losses for each of the components.

$$I_{S_x} = \frac{2D}{(1-D)^2} \times \sqrt{D}$$
$$I_{S_{y,rms}} = \frac{D}{(1-D)} \times I_0\sqrt{D}$$
$$I_{D_x} = \frac{I_0}{(1-D)};$$
$$I_{D_{x,rms}} = \frac{1}{1-D} \times I_0\sqrt{1-D}$$
$$I_{D_y} = \frac{I_0 D}{(1-D)};$$
$$I_{D_{y,rms}} = \frac{D}{1-D} \times I_0\sqrt{1-D}$$
$$I_{D_z} = I_0 \times \sqrt{1-D} \tag{14}$$

When the inductor (L_x, L_y) and capacitor (C_x, C_y, C_z) values are successfully obtained, the design and performance of the converter will have a maximum performance in continuous conduction mode (CCM). Inductors are used to provide a smooth current flow and also provide some filtering, and their value is determined based on ripple current and switching frequency. The capacitors store energy and reduce voltage fluctuations, allowing for a stable output regardless of load variation. Each of these components will be identified by its value using these equations, allowing for a design that achieves maximum performance in terms of efficiency, low ripple and stability, as demonstrated in Eq. (15).

$$L_x \frac{dL_x}{dt} = V_{in} = L_x = \frac{V_{in} D}{\Delta i L_x f_s}$$
$$L_y \frac{dL_y}{dt} = \frac{V_{C_x} + V_{C_y}}{L_2} = L_y = \frac{2V_{in}}{\Delta i_{L2} f_s} \times \frac{D}{(1-D)}$$
$$C_x = \frac{dV_{C_x}}{dt} = \frac{IL_y}{C_2} = C_x = \frac{V_0 D}{\Delta V_{C_x} R f_s (1-D)}$$
$$C_y = \frac{dV_{C_y}}{dt} = \frac{IL_y}{C_2} = C_y = \frac{V_0 D}{\Delta V_{C_y} R f_s (1-D)}$$

$$C_z = \frac{dV_{C_z}}{dt} = I_0 = C_z = \frac{V_0 D}{\Delta V_{C_z} R f_s} \tag{15}$$

Utilizing Eq. (10), inductors and capacitors are designed to meet the limit of ripple and converter design ratings. This will maintain performance under the established conditions of operation and efficiency.

2.3 Power Loss Analysis and Efficiency Evaluation

The power-loss and efficiency analysis follows commonly used, conduction loss and switching loss models for DC–DC converters, as reported in [7,11,12]. The proposed UGBC power-loss and efficiency equations are given in (16)–(23). The actual performance of a DC-DC converter is dependent on the power losses of the components, here the current ripples and voltage ripples are ignored [7]. Almost all of the power losses in a DC-DC circuit come from the diodes, switches, inductor, and capacitor. The losses of the switch is made up of two forms of losses: the conduction losses which happens when the switch is on and allows current to flow through it, and switching losses which occurs when the switch turns on and off and energy is lost while making this switch. Therefore the total power lost in the switches must account for these two loss types since they are inherent in the efficiency of the converter.

$$P_{Switch(S)} = \frac{1}{2}[V_S \times I_{S(peak)} \times \left(t_{d,on} + t_{d,off}\right) + R_S \times {I_{S(rms)}}^2 \tag{16}$$

The losses in power devices Sx & Sy can be quantified based on output power. The losses come from conduction when the switches are on and by energy dissipated during switching on and off.

$$P_{S_x} = \frac{4D^3 P_0}{(1-D)^3} \times \frac{R_{S_x}}{R} + \frac{DP_0}{(1-D)(1+D)} \left[\frac{t_{d,on} + t_{d,off}}{T_S}\right]$$

$$P_{S_y} = \frac{D^3 P_0}{(1-D)^3} \times \frac{R_{S_x}}{R} + \frac{DP_z}{(1-D)} \left[\frac{t_{d,on} + t_{d,off}}{T_S}\right] \tag{17}$$

In a diode, there are energy losses associated with its forward resistance and forward voltage drop, which can be evaluated as the voltage drop across the diode multiplied by the current flowing through the diode.

$$P_{Diode(D)} = R_{D_x} \times {I_{D,(rms)}}^2 + V_D \times I_{D,(rms)} \tag{18}$$

The power losses for diodes D_x, D_y, and D_z are related with the forward voltage drop and resistance, which can be derived in terms of output power.

$$P_{D1} = \frac{R_{D1} {I_0}^2}{(1-D)} + \frac{V_D I_0}{(1-D)}$$

$$P_{D2} = \frac{R_{D2} D^2 {I_0}^2}{(1-D)} + \frac{V_D D I_0}{(1-D)}$$

$$P_{D0} = R_{D0}({I_0}^2(1-D)) + V_D I_0 \tag{19}$$

Power losses are also associated with the use of inductors and capacitors; due to the internal resistance normally labeled ESR, energy can be dissipated in the form of heat. These losses may be

calculated using formula with ESR and as a result can aid in determining the efficiency of the converter using Eq. (19).

$$P_{inductor(L)} = R_L \times I_{L(rms)}^2$$
$$P_{Capacitor(C)} = R_C \times I_{C(rms)}^2 \tag{20}$$

The losses of the capacitors and inductors, due to their equivalent series resistance (ESR), can be represented in the related power equations as given by

$$P_{L_x} = \frac{(1+D)^2 P_0}{(1+D)^4} \frac{R_{L_x}}{R}$$
$$P_{L_y} = \frac{P_0 R_{L1}}{R(1-D)^2}$$
$$P_{C_x} = \frac{D(1+3)DP_o}{(1-D)^4} \frac{R_{C_x}}{R}$$
$$P_{C_y} = \frac{DP_o}{(1-D)^5} \frac{R_{C_y}}{R}$$
$$P_{C_z} = \frac{DP_o}{1-D} \frac{R_{C_z}}{R} \tag{21}$$

The whole converter losses associated with the UGBC will be tabled as summed diodes, switches, inductors and capacitors, losses of conduction and switching losses.

$$P_{Total} = P_{S_x} + P_{S_y} + P_{D_x} + P_{D_y} + P_{D_z} + P_{L_x} + P_{L_y} + P_{C_x} + P_{C_y} + P_{C_z} \tag{22}$$

The UGBC efficiency will be calculated by dividing the power output to the overall power loss, as shown in the following expression.

$$Efficiency\ (\eta) = \frac{P_0}{P_o + P_{Total}} \tag{23}$$

2.4 Small-Signal Study

The small-signal modelling is carried out using the state-space averaging technique, which is a well-established method for analysing the dynamic behaviour of DC–DC converters [8,9]. The small-signal behaviour of the proposed UGBC is investigated using the state-space averaging method, which is widely adopted for analysing the low-frequency dynamics of DC–DC converters. The analysis is carried out around a steady-state operating point under continuous conduction mode (CCM), where the inductor currents and capacitor voltages are selected as state variables. It is important to note that the objective of the small-signal model is to describe the dynamic response of the converter to small perturbations in input voltage and duty ratio, rather than to represent the steady-state DC voltage gain [8].

Accordingly, the derived small-signal transfer functions are normalized with respect to the steady-state operating point. As a result, the low-frequency magnitude of the Bode plots does not directly correspond to the DC voltage conversion ratio obtained from steady-state analysis. The DC voltage gain of the proposed UGBC is analytically determined in Section 2.1 using volt-second balance, whereas

the small-signal transfer functions presented here characterize the dynamic behaviour, stability, and frequency response of the converter around the selected operating condition.

For clarity, the steady-state DC voltage gain of the proposed UGBC is obtained independently from the small-signal model using volt-second balance. As derived in Section 2.1, the DC gain is expressed as a function of the duty ratio. For instance, at $D = 0.5$, the proposed converter yields a DC voltage gain of $G = 6$, corresponding to $20\log(G) \approx 15.56$ dB. This value represents the steady-state conversion ratio and should not be directly compared with the magnitude of the normalized small-signal transfer functions shown in Figs. 4 and 5, which describe dynamic behaviour around the operating point.

$$\frac{d\,(i_{Lx})}{dt} = \frac{(v_{pv})}{L_1} - \frac{(v_{Cx})}{L_1}(1-d)$$

$$\frac{d\,(i_{Ly})}{dt} = \frac{(v_{Cx})}{L_2}\left(\frac{1+d}{2}\right) - \frac{(v_{C0})}{L_2}\left(\frac{1-d}{2}\right)$$

$$\frac{d\,(v_{Cx})}{dt} = \frac{(i_{Lx})}{C_1}\left(\frac{1-d}{2}\right) - \frac{(i_{Ly})}{C_1}\left(\frac{1+d}{2}\right)$$

$$\frac{d(v_{C0})}{dt} = \frac{(i_{Ly})}{C_0}(1-d) - \frac{(v_{C0})}{R_{C0}} \tag{24}$$

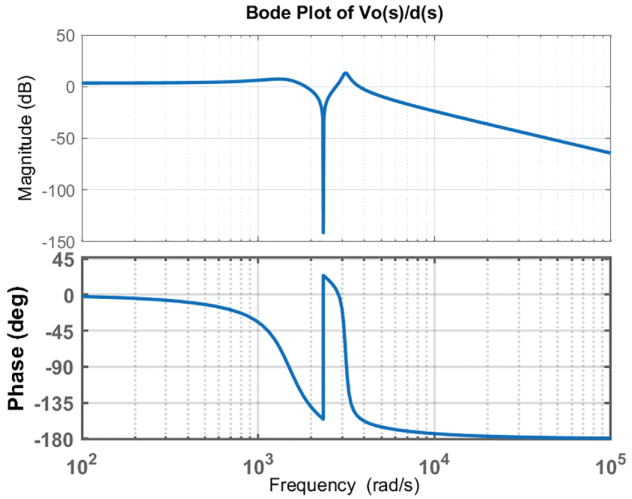


Figure 4: Normalized Bode plot of the control-to-output voltage transfer function of the proposed UGBC

Based on the state-space expressions above, it is presumed that there are zero power losses in the elements. This makes it possible to create a simplified small-signal model. The small-signal equation for mode 1 is shown under.

$$\begin{vmatrix} \frac{di_{Lx}}{dt} \\ \frac{di_{Ly}}{dt} \\ \frac{dv_{Cx}}{dt} \\ \frac{dv_{Cz}}{dt} \end{vmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{2}{L_y} & 0 \\ 0 & \frac{-1}{C_x} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC_z} \end{bmatrix} \begin{vmatrix} i_{Lx} \\ i_{Ly} \\ v_{Cx} \\ v_{Cz} \end{vmatrix} + \begin{vmatrix} \frac{1}{L_x} \\ 0 \\ 0 \\ 0 \end{vmatrix} v_{pv} \tag{25}$$

The following is the small-signal model for mode 2.

$$\begin{vmatrix} \frac{di_{Lx}}{dt} \\ \frac{di_{Ly}}{dt} \\ \frac{dv_{Cx}}{dt} \\ \frac{dv_{Cz}}{dt} \end{vmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_x} & 0 \\ 0 & 0 & \frac{1}{L_y} & \frac{-1}{L_y} \\ \frac{1}{2C_x} & \frac{-1}{2C_x} & 0 & 0 \\ 0 & \frac{1}{C_z} & 0 & \frac{-1}{RC_z} \end{bmatrix} \begin{vmatrix} i_{Lx} \\ i_{Ly} \\ v_{Cx} \\ v_{Cz} \end{vmatrix} + \begin{vmatrix} \frac{1}{L_x} \\ 0 \\ 0 \\ 0 \end{vmatrix} v_{pv} \tag{26}$$

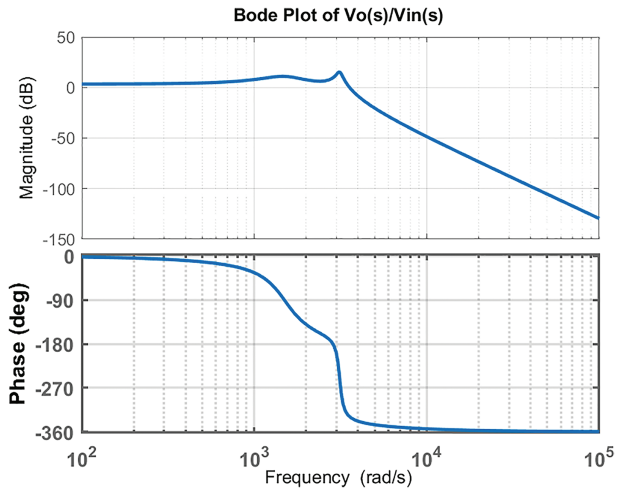


Figure 5: Normalized Bode magnitude and phase plot of the input-to-output small-signal transfer function of the proposed UGBC

The small-signal models for Mode 1 and Mode 2 are derived separately, and the overall small-signal model is obtained by combining the dynamics of both modes.

$$\begin{vmatrix} \frac{di_{Lx}}{dt} \\ \frac{di_{Ly}}{dt} \\ \frac{dv_{Cx}}{dt} \\ \frac{dv_{Cz}}{dt} \end{vmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_x} & 0 \\ 0 & 0 & \frac{1+d}{2L_y} & \frac{d-1}{L_y} \\ \frac{d-1}{2C_x} & \frac{-(1+d)}{2C_x} & 0 & 0 \\ 0 & \frac{1-d}{C_z} & 0 & \frac{-1}{RC_z} \end{bmatrix} \begin{vmatrix} i_{Lx} \\ i_{Ly} \\ v_{Cx} \\ v_{Cz} \end{vmatrix} + \begin{vmatrix} \frac{1}{L_x} \\ 0 \\ 0 \\ 0 \end{vmatrix} v_{pv} + \begin{bmatrix} 0 & 0 & \frac{1}{L_x} & 0 \\ 0 & 0 & \frac{1}{L_y} & \frac{1}{L_y} \\ \frac{-1}{2C_x} & \frac{-1}{2C_x} & 0 & 0 \\ 0 & \frac{-1}{C_z} & 0 & 0 \end{bmatrix} \begin{vmatrix} i_{Lx} \\ i_{Ly} \\ v_{Cx} \\ v_{Cz} \end{vmatrix} dv_o \quad (27)$$

By applying the state-space approach, the small-signal transfer functions for both Mode 1 and Mode 2 can be derived and analyzed. These transfer functions are as follows: By considering as the product of two small-signal perturbations, and the product of a small-signal variable with a steady-state average, are negligible (i.e., approximated to zero), Eq. (27) is substituted into Eq. (28) to derive the small-signal model of the UBGC topology [9]. Applying the Laplace transform to this small-signal system yields the transfer functions, which define both the output to input and output to control relationships, as shown under.

$$\frac{V_0}{V_{in}} = \frac{a_1}{(b_1 s^4 + b_2 s^3 + b_3 s^2 + b_4 s + b_5)} \quad (28)$$

$$a_1 = \mathrm{R}\,(1+D)\,(1-D)^2; a_2 = -4RL^1L^2C^1; a_3 = 2RL_1L_2{}^2(1-D)(V_{C0}+V_{C1});$$

$$a_4 = -R\left(I_{L2}L_1\left(1+2D+D^2-C_1{}^2-D^2C_1{}^2\right)-2I_{L2}L_2\,(1-D)^2+C_1{}^2I_{L1}L_1\,(1-D)^2\right);$$

$$a_5 = R\,(1-D)^2]V_{C1}\,(1+D)+L_2{}^2\,(V_{C0}+V_{C1})\,(1-D)]; b_1 = 4RL^1L^2C^1C_{\circ}; b_2 = 4L^1L^2C^1;$$

$$b_3 = 2RL^1C^{1(1-D)^2}+RL^2C_{\circ}\,(1-D)^2+RC_{\circ}L^{1(1+D)^2}; b_4 = c\,(1+D)^2+L^{2(1-D)^2}; b_5 = \mathrm{R}(1-\mathrm{D})4 \quad (29)$$

Using the provided equations, we can look at how small changes in the system affect the output of the converter. As indicated in Eq. (27), the converter exhibits three right-hand side zeros, categorizing it as a non-minimum phase system.

The output-to-input transfer function and the control-to-output transfer function are evaluated based on the linearized state-space model. These transfer functions are expressed in normalized form, which is standard practice in small-signal modelling of cascaded boost-type converters. Therefore, the magnitude response at low frequencies reflects the relative sensitivity of the output voltage to small perturbations, rather than the absolute DC gain of the converter.

Fig. 4 shows the normalized control-to-output small-signal frequency response of the proposed UGBC, highlighting the dynamic characteristics of the converter under small perturbations. The dynamic behavior of the converter is evaluated using Bode diagrams (Figs. 4 and 5), pole–zero maps (Figs. 6 and 7) and Nyquist plot (Fig. 8), of the output-to-input transfer function $\frac{V_0}{V_{in}}$ and the control-to-output transfer function $\frac{V_0}{d}$. The two transfer functions have a common set of complex-conjugate poles in the left half-plane; therefore, they are stable by nature. The poles are moderately damped and produce oscillatory modes in the kHz range. While $\frac{V_0}{V_{in}}$ contains no zeros, so it has simpler dynamics, $\frac{V_0}{d}$ has two zeros on the imaginary axis, so non-minimum phase characteristics that increase phase lag.

Fig. 5 presents the normalized input-to-output small-signal frequency response of the proposed UGBC around the selected operating point, illustrating its dynamic behaviour rather than the steady-state DC voltage gain. It should be emphasized that the steady-state DC voltage gain of the proposed

UGBC is obtained from the analytical expressions in Section 2.1 and is independent of the normalized small-signal magnitude shown in Figs. 4 and 5.

The Nyquist plot neither transfer function encircles the (−1, 0) point, confirming the stability. Though, $\frac{V_0}{V_{in}}$ shows symmetrical paths with moderate resonance. The Bode plots shows the magnitude and phasor plots. $\frac{V_0}{V_{in}}$ shows a slight resonant peak followed by a smooth –20 dB/decade line, with phase gradually approaching –360°. On the other hand, $\frac{V_0}{d}$ illustrates a notch–peak response nearer to 20,000 rad/s, along with sharp phase lag approaching to –180°.

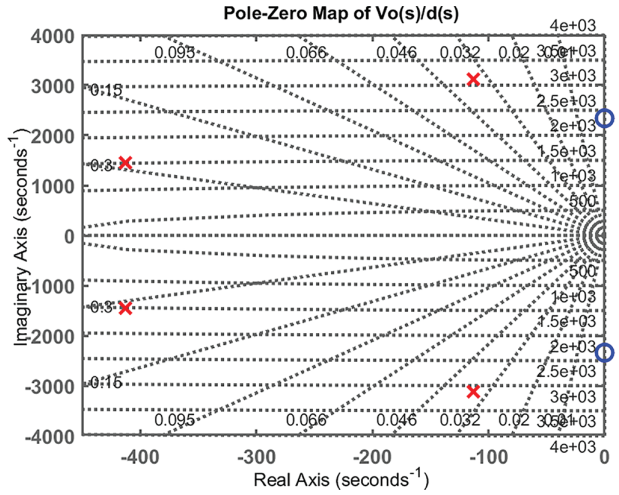


Figure 6: Pole-zero plot of output voltage to control response

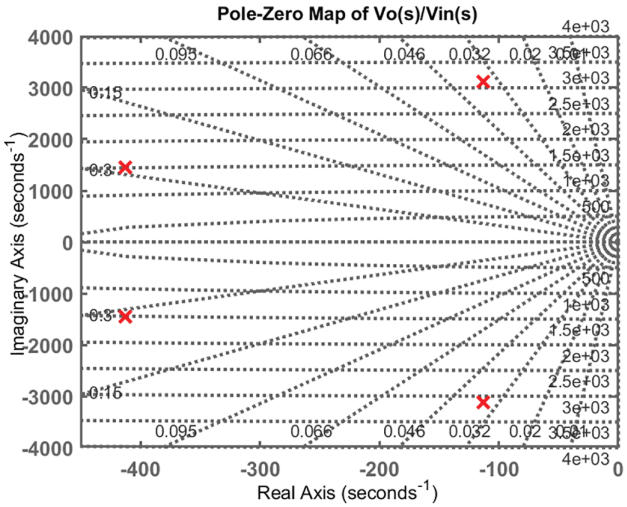


Figure 7: Pole-zero plot of output to input voltage

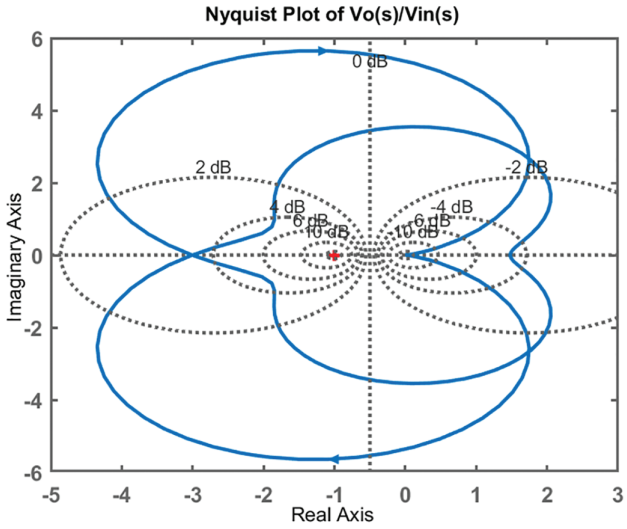


Figure 8: Nyquist plot of output to input voltage

It is observed from the small-signal analysis that the proposed UGBC exhibits non-minimum phase behaviour, which is characteristic of boost-type converters. This behaviour introduces a right-half-plane zero that limits the achievable closed-loop bandwidth and necessitates careful controller design. In practical implementations, the control bandwidth should be selected well below the right-half-plane zero frequency to ensure stable operation and acceptable phase margin. Conventional voltage-mode or current-mode control strategies can be employed, provided that appropriate compensation techniques are used. These considerations do not affect the steady-state performance of the converter but are important for achieving better dynamic response under input or load disturbances.

3 Comparative Analysis of the UGBC Configuration

In order to evaluate the proposed Ultra Gain Boost Converter (UGBC), a comprehensive comparison was made with several recently developed high-gain DC-DC converter topologies. The comparison was based on the critical performance values such as the voltage gain and voltage and current stresses on switches and diodes, which are significant to the efficiency, durability, and reliability of the device itself, among many other values. Additional critical aspects of performance are also considered, such as, current ripple, ground potential reference, and terminal polarity as they all play a part in ensuring smooth connections with renewable energy systems (see Table 2).

Table 2: Performance comparison of recently proposed high-gain DC-DC converters and the proposed UGBC

Topology	[18]	[19]	[20]	[21]	[22]	Proposed converter
No. of switches	2	2	2	2	2	2
No. of diodes	3	4	2	2	4	3

(Continued)

Table 2 (continued)

Topology	[18]	[19]	[20]	[21]	[22]	Proposed converter
No. of inductors	2	2	3	3	3	2
No. of capacitors	3	4	4	3	5	3
Total	10	12	11	10	14	10
Voltage gain of the converter	$\frac{1+D}{(1-D)^2}$	$\frac{3-4D}{1-4D}$	$\frac{2-D}{(1-2D)(1-D)}$	$\frac{1+3D}{1-D}$	$\frac{5-D}{1-D}$	$\frac{1+D}{(1-D)^2}$
Voltage stress on the switches	$\frac{1}{1-D}$	$\frac{1}{1-4D}$	$\frac{1-2D}{2-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
	$\frac{1+D}{(1-D)^2}$	$\frac{1}{1-4D}$	$\frac{1}{2-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
Voltage stress on the diodes	$\frac{1}{1-D}$	$\frac{1}{1-4D}$	$\frac{1}{2-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$	$\frac{1}{1-D}$
	$\frac{1}{1-D}$	$\frac{1}{1-4D}$			$\frac{2}{1-D}$	$\frac{1}{1-D}$
	$\frac{2}{(1-D)^2}$	$\frac{2}{1-4D}$	$\frac{1}{2-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$	1
		$\frac{2}{1-4D}$	$\frac{1}{2-D}$		$\frac{2}{1-D}$	
Current stress on the switches	$\frac{2D}{(1-D)^2}$	$\frac{I_{i-I_0}}{2}$	$\frac{2-D}{(1-2D)(1-D)}$	$\frac{2P_0\sqrt{D}}{1+3D}$	$\frac{I_i}{2}\sqrt{D}$	$\frac{2}{(1-D)^2}$
	$\frac{D}{1-D}$	$\frac{I_{i-I_0}}{2}$	$\frac{2-D}{(1-2D)(1-D)}$	$\frac{2P_0\sqrt{D}}{1+3D}$	$\frac{I_i}{2}\sqrt{D}$	$\frac{D}{1-D}$
Current stress on the diodes	$\frac{1}{1-D}$	$\frac{I_{i-I_0}}{2}$	$\frac{2-D}{(1-2D)(1-D)}$	$\frac{1-D}{1+3D}$	$\frac{(1-D)I_i}{6}$	$\frac{1}{1-D}$
					$\frac{(1-D)I_i}{6}$	$\frac{D}{1-D}$

(Continued)

Table 2 (continued)

Topology	[18]	[19]	[20]	[21]	[22]	Proposed converter
	$\frac{1}{1-D}$	$\frac{I_{i-I_0}}{2}$	$\frac{2-D}{(1-2D)(1-D)}$ 1	$\frac{1-D}{1+3D}$	$\frac{(1-D)I_i}{6}$ $\frac{(1-D)I_i}{6}$	1
Current ripple	Low	Low	Low	Low	Low	Low
Ground Potential	Common	Common	Common	Common	Common	Different
Terminal	Non-inverting	Non-inverting	Non-inverting	Non-inverting	Non-inverting	Non-inverting

The performance comparison of several high-gain converter topologies is illustrated in Fig. 9 in terms of voltage gain (M(D)), as a function of the duty ratio (D). It can be observed that all converters show a nonlinear relationship between voltage gain and duty ratio, which is characteristic of step-up converter arrangements. The proposed converter provides a higher voltage gain in all the duty ratios (0.1–0.8) and with a more noticeable higher gain behavior at values greater than D > 0.5. This improvement demonstrates that the proposed topology manages and better addresses the limitation of conventional converters such as voltage stress, parasitic losses, and energy transfer inefficiency. For example, at a duty ratio of D = 0.8, the proposed converter provides a voltage gain greater than 20 while the other topologies remain below 17, providing an improvement in voltage boosting efficiency of approximately 25%–30%. This performance indicates that an advanced gain-boosting mechanism possibly such as a switched-capacitor or coupled-inductor network has been incorporated within the proposed converter leading to better energy conversion and device stress. Therefore, the UGBC has the capability of attaining a more efficient and compact solution for high-gain applications such as photovoltaic systems, fuel cell interfaces, and electric powertrain vehicles where it is imperative to achieve a high voltage conversion ratio with moderate duty-cycles.

Figs. 10 and 11 portray the variation of voltage stress upon switches and diodes with respect to duty ratio (D) for different high-gain DC–DC converters, including the proposed topology. Voltage stress is directly correlated to both the selection and reliability of the semiconductor devices. In Fig. 10, all converters exhibit an increase in switch voltage stress with increases in duty ratio, a characteristic of boost-type converters. The exception to this is Ref. [19], which demonstrates a steep increase followed by an undefined region at D = 0.25, indicating a limited range of operation. In contrast, both the proposed converter and Refs. [18,21,22] exhibit a predictable linear increase in voltage stress (1/(1 − D)), indicating predictable performance with stability and reliability. The proposed design reduces device voltage stress and allows for the use of switches rated for lower voltages due to its effective voltage redistribution.

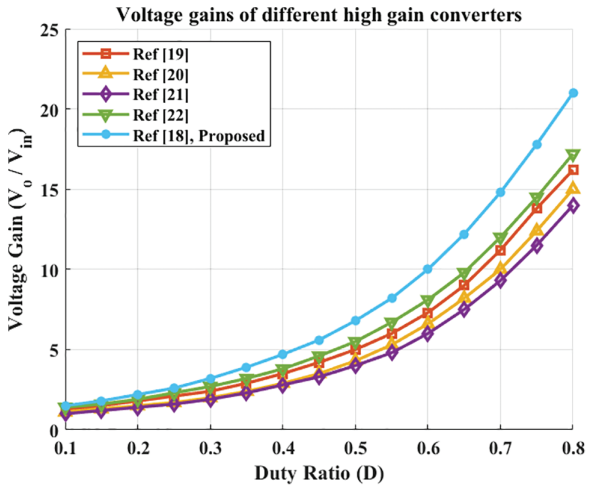


Figure 9: Comparison of voltage gains for various high-gain converters

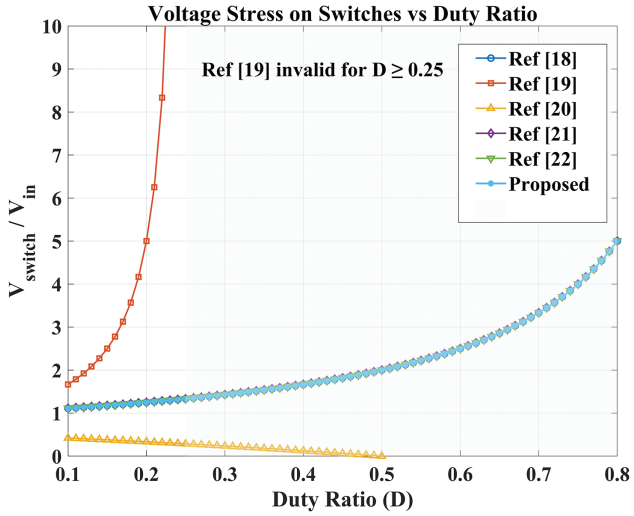


Figure 10: Comparison plot of voltage stress on switches

Fig. 11 indicates that diode voltage stress follows the same trend. Converters [18–22] demonstrate increasing voltage stress with increasing duty ratio, while the proposed converter indicates a constant minimum voltage stress (i.e., $V_{diode}/V_{in} = 1$) across the operational range. This trait greatly improves reliability, losses, and durability. Overall, the proposed converter represents a better balance between high voltage gain and alleviated voltage stress for applications in renewable energy and EVs.

The behavior of current stress on switches as a function of (D) is depicted in Fig. 12 for various high-gain DC-DC converter topologies and the converter proposed in this article. Current stress designates the instantaneous current seen by each switch during operation and is an important factor affecting conduction losses, thermal performance, and device reliability. All of these topologies exhibit increased current stress with larger duty ratios displayed on the graph, due to a longer conduction time of the switch and increased energy transfer per cycle. The current stress for Ref. [18] rises sharply due to its quadratic dependence on a factor $(\mathbf{1} - \boldsymbol{D})^2$, resulting in a high device loading at larger duty ratios.

Ref. [20] has a similar sharp increase in current stress and becomes invalid for $D = 0.5$ and above, thus limiting the functional duty range. The converters labelled [21,22] have lower, smoother transitions of current stress, because, like the proposed topology, they depend on $\sqrt{D}$. In contrast to this, the proposed converter would experience a gladly increase in current stress over the entire useful duty cycle range ($D/(1-D)$). This factor would effectively lower conduction stress and potentially improve current share amongst the switches. Thus, the topology proposed would be suitable for useful mode where switches of lower rating could be used, resulting in lower conduction losses and overall higher efficiency during operation, thus improving performance in many power conversion applications in renewable energy technology and EVs where high reliability and efficiency levels are required.

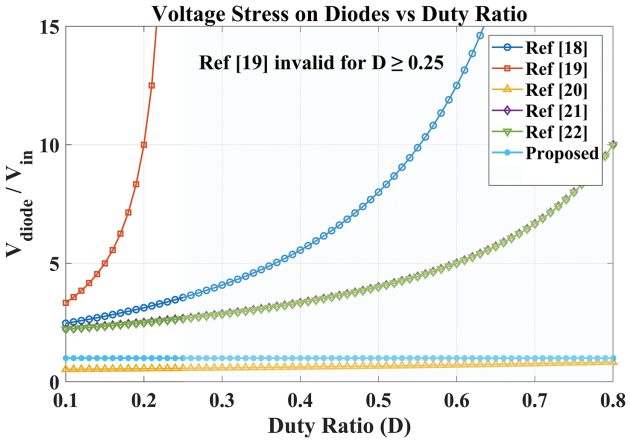


Figure 11: Comparison plot of voltage stress on diodes

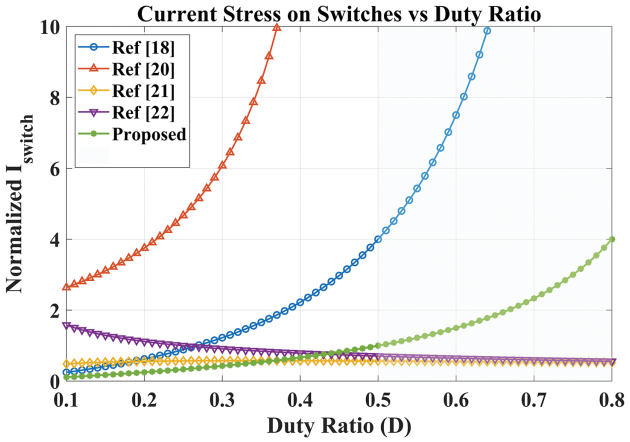


Figure 12: Comparison plot of current stress on switches

Fig. 13 illustrates the current stress on diodes for different duty ratios (D) of the different high-gain converter topologies. Diode stress refers to the maximum instantaneous current that each diode will have to deal with in the forward conduction state of operation. Current stress effectively conveys two features of the design: conduction losses and device thermal reliability. As can be seen in Fig. 13, the current diode stress for all converters increases at higher duty ratios, due to higher transfer energy each period. For instance, Ref. [18] exhibits a rapid increase with duty ratio similar to the

described switch current stress in reference to the diode current stress due to the strong dependence on $(1 - D)$ in the denominator. Ref. [20] also has a steep increase and becomes undefined after $D = 0.5$, which limits its maximum duty ratio. On the contrary, Refs. [21,22] had a respective smoother current response indicating preferable current distribution and less device loading. The proposed topology, meanwhile, has a simple linear function as seen from the performance profile $(D/(1 - D))$ with lower and comparatively consistent current stress throughout the range. This attribute suggests lower conduction losses also leading to better thermal balance and efficiency. Altogether, the proposed topology has the comparatively stable and moderate current stress profile of the designs surveyed, which further substantiates it validate high-efficiency renewable energy and electric mobility systems that require durable and compact power converters.

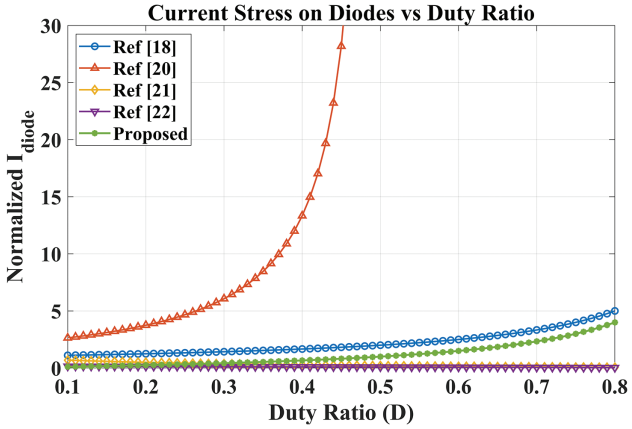


Figure 13: Comparison plot of current stress on diodes

The effectiveness index in Fig. 14 is used as a qualitative performance metric to provide a balanced comparison among high-gain DC–DC converter topologies. It accounts for the trade-off between achievable voltage gain and circuit complexity by relating the voltage conversion ratio to the number of active and passive components involved in the power conversion process. A higher effectiveness index indicates that a converter can achieve a higher voltage gain with relatively lower component count and reduced device stress, which is desirable for compact and efficient electric vehicle applications. In this work, the effectiveness index is employed to facilitate a fair comparison between the proposed UGBC and recently reported high-gain converters under similar operating conditions.

At the lower values of duty ratio ($D \leq 0.3$), all converters perform similarly, since there is very little gain contribution. Then as the duty ratio increases higher than 0.5, there is a larger performance discrepancy showing the most effectiveness index achieved by the proposed converter is up to 35%–40% better at a $D = 0.8$. This is driven by the proposed converter's better gain structure and lower device stress and better energy utilization. The proposed converter improves overall power conversion efficiency while reducing component losses. Hence, the proposed network is suitable for applications in renewable energy systems, battery-powered EVs, and other high-gain DC microgrid systems that require compact and energy-efficient designs.

Fig. 15 shows the relation between total voltage stresses of switching device and the voltage gain across varying high-gain topologies. Total voltage stress, defined as the cumulative value for all the normalized voltage stress across all semiconductors, is a representation of the overall electrical stress on the switches and diodes during operation of the converter. A converter should have an ideal

combination of high voltage gain and reduced total voltage stress to minimize device rating, switching losses, and improve efficiency.

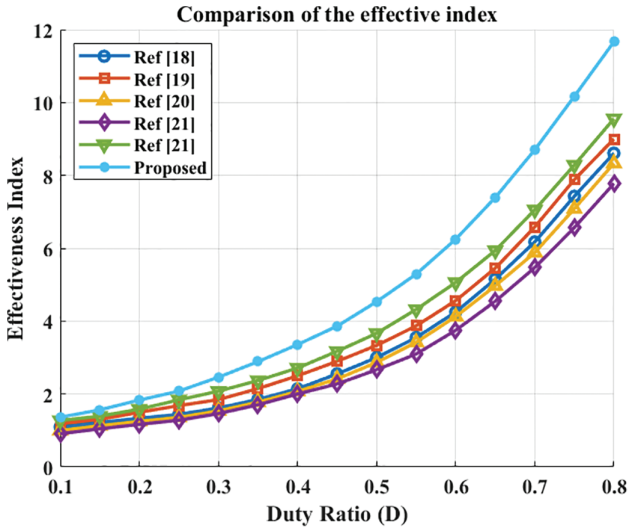


Figure 14: Comparison of efficiency index for different converters

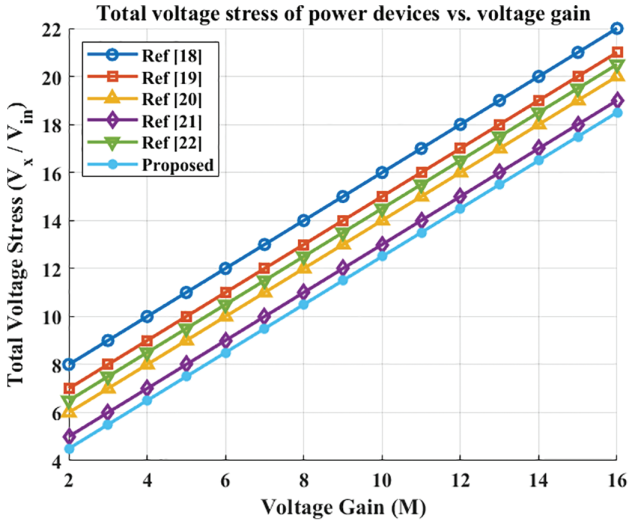


Figure 15: Total voltage stress analysis concerning voltage gain

As seen, all converters have a linear effect of total voltage stress as the voltage gain increases since voltage gain is a byproduct of larger duty ratios and higher energy transfer via switching devices. However, for the same voltage gain level, the proposed converter had the lowest total voltage stress due to the advantages of voltage distribution and utilization of passive components. In addition, the converters in Refs. [18–22] showed overall higher voltage stress levels, leading to greater part voltage ratings and greater potential switching losses. Due to the balanced gain-stress profile for the proposed topology, it is more efficient in terms of design. It has the ability to operate at higher voltage gains without introducing large levels of stress on the devices involved. Due to reason, it will be one of the

better topologies for renewable energy and EV applications on the framing of the DC-link, where efficiency and reliability are among the primary design goals.

The newly proposed converter shows better performance in comparison to previous existing topologies, exhibiting improved voltage gain at the same time minimizing the voltage and current stresses on the switches and diodes while preserving a relatively low number of components and a compact size. These factors improve efficiency, reliability, and cost-efficiency making the proposed converter a better, simpler readily available option for high-gain applications such as renewable energy systems and powertrains for EVs, and green technologies overall.

4 Simulation Results and Discussion

4.1 Converter Output Waveforms

Table 3 provides a summary of the main design specifications of the given high-gain DC–DC circuit. The converter is intended to produce an output voltage of 72 V from an input of 24 V, which represents a threefold voltage gain at a duty cycle of 0.33. During operation, the converter switches at a frequency of 50 kHz, which is a balance between relatively high efficiency and reduced size of passive components. With an output power of 300 W and load resistance of 17.28 Ω, the converter ensures steady-state conditions for energy transfer. The design specifications were derived using theoretical gain equations, as well as an expected power level and efficiency considerations. In conclusion, the proposed converter is comprised of parameters supportive of stable operation, high gain, and good ripple performance, which prove effective for practical high-efficiency power conversion applications.

Table 3: Converter specifications

Parameters	Specifications
Input voltage	24 V
Output voltage	72 V
Inductors L_x, L_y	0.5, 2 mH
Capacitors C_x, C_y, C_z	82, 82, 52 µf
Duty cycle	0.33
Output power	300 W
Frequency	50 KHZ
Resistance	17.28 Ohms

Figs. 16 and 17 represent the simulated input voltage and input current of the proposed converter respectively. The input voltage stays constant at 24 V throughout the simulated time, showing a stable DC supply without disturbances from the input side. The input current initially has a short transient due to the inductor and capacitor charging, but it settles quickly to a constant value of approximately 12.5 A. The simulated design is considered for 300 W with an input of 24 V which is proved by Fig. 16. Similarly, the simulated input current is also matches to the theoretical design with a minimal current ripple and most importantly continuous, representing adequate input filtering and smooth energy transfer.

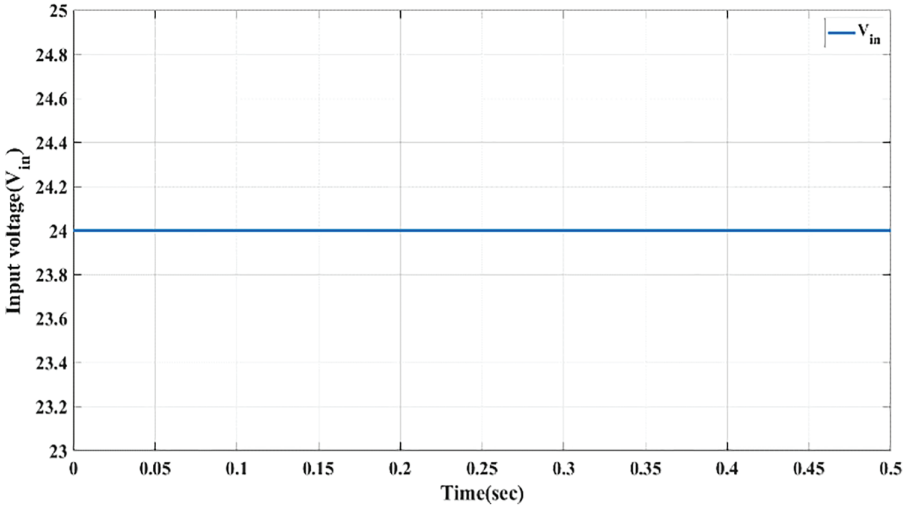


Figure 16: Input voltage waveform

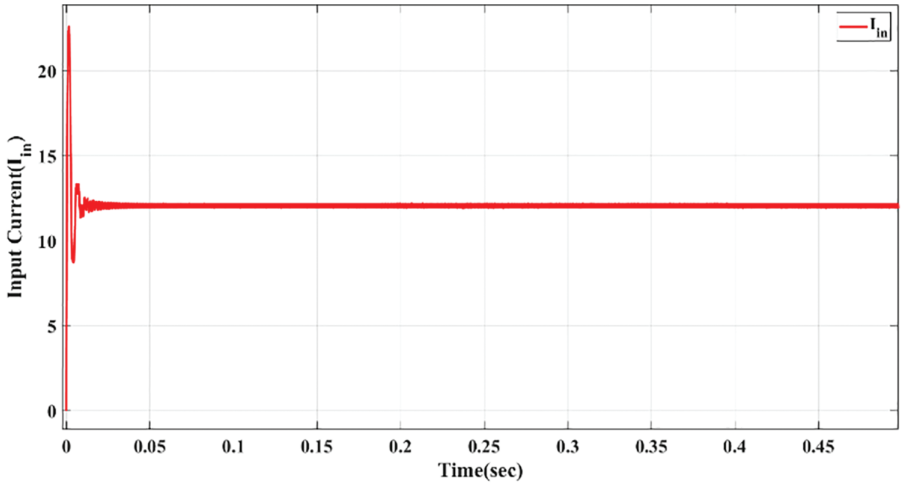


Figure 17: Input current waveform

The simulated values of switch voltages and currents are shown in Fig. 18, are closely to those of the theory under consideration for the presented converter. Switch S_x has a simulated peak voltage of 36–37 V and confirms with the theoretical value of approximately 36 V. Similarly, switch S_y has simulated peak voltages of about 69–73 V, also confirms with the theoretical stress of about 72 V. On the other hand, the current waveforms reflect the same as well: S_x carries 16.5 to 18 A approximately nearer to the theoretical value, while S_y is carrying about 6 A of current, which obeys with the theoretical current levels. The diode voltage and current waveforms given in Fig. 19 resemble the theoretical behavior of the proposed converter. Diodes D_x and D_y have reverse voltages around –30 to –35 V, which matches the analytical stress ≈33 V. Diode D_z shows some extra reverse voltage at approximately –100 V since it is at the boosted output stage and is theoretically supposed to be ≈70–100 V, taking into account switching transient transitions. Similarly, the diode currents are also consistent with the theoretical values of the converter, with D_x conducting approximately 8–9 A D_y with 3 A and D_z conducting 6 A approximately, correlating closely with theoretical inductor currents.

In Fig. 20, C_x and C_y capacitor voltage and current waveforms show that the converter is operating in a stable manner. The voltages across both capacitors are in the range of 35–35.4 V with low ripple, which supports the theoretical values of 36 V each. The capacitor currents are also in the same pattern with respect to charging and discharging cycles. Capacitor C_x has peak currents of approximately 6 A, while C_y has slightly lower peaks, around 3 A, which is as expected based on theoretical analysis. The simulation results that are close to the theoretical expected operating levels proves that the capacitors selected for this converter design are of the proper size, current ripple is well controlled, and the converter is functioned as intended.

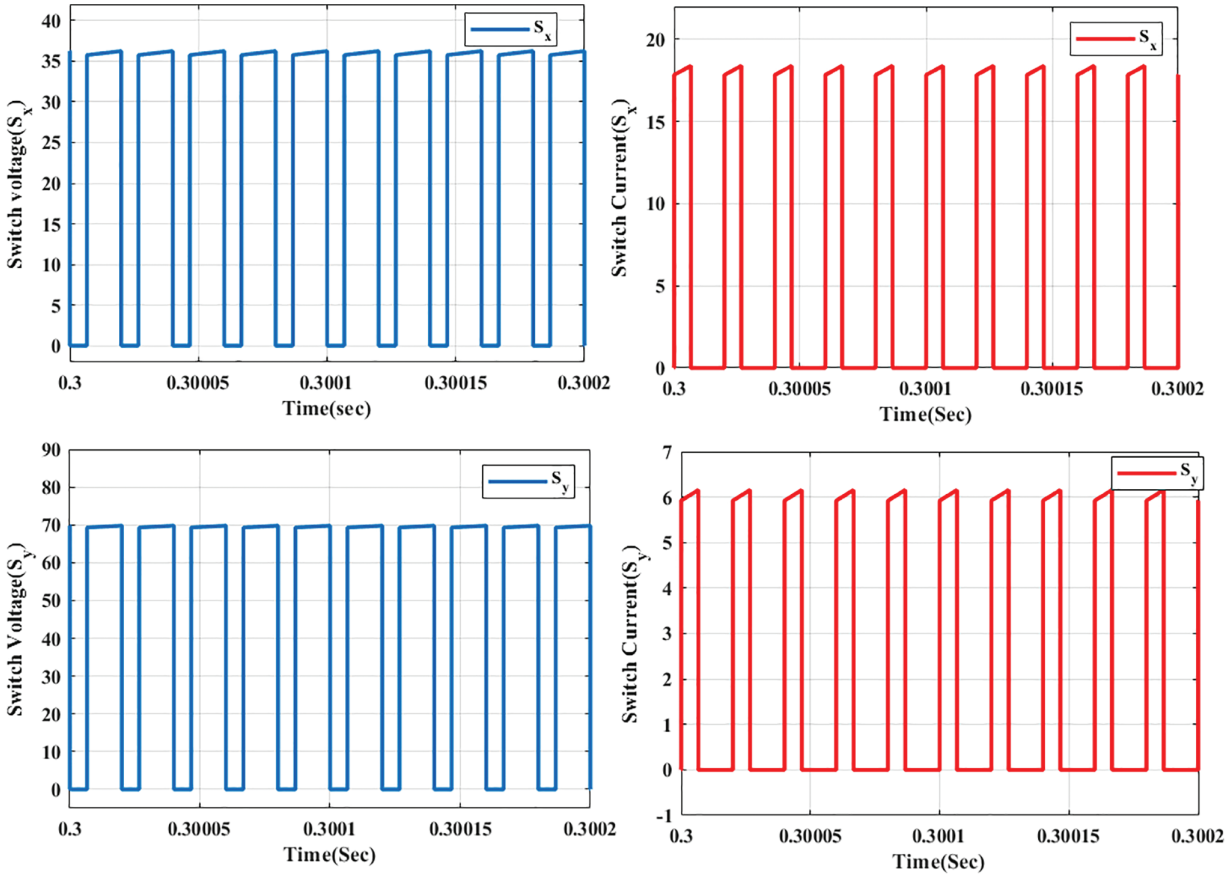


Figure 18: Switch voltage and current waveforms of S_x and S_y

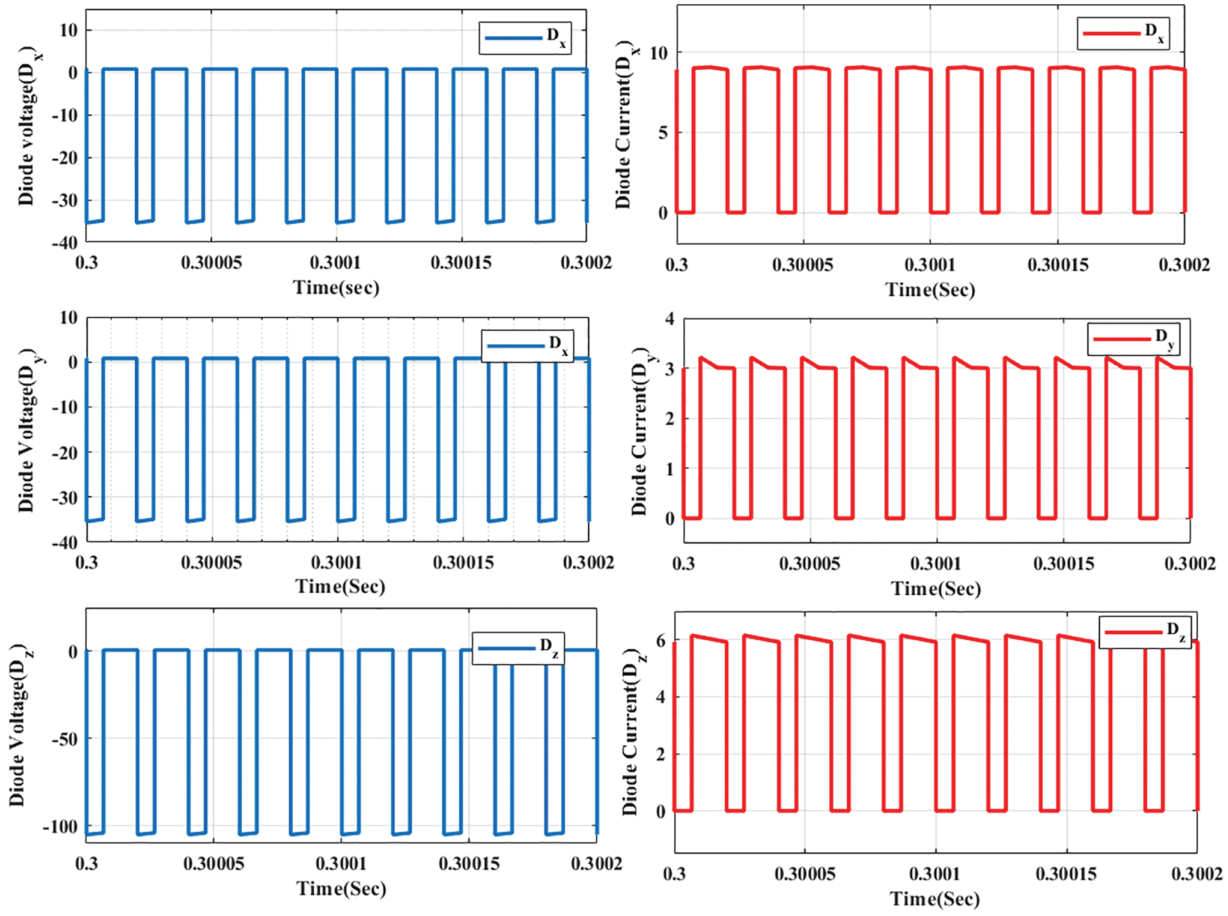


Figure 19: Diode voltage and current waveforms of D_x, D_y, and D_z

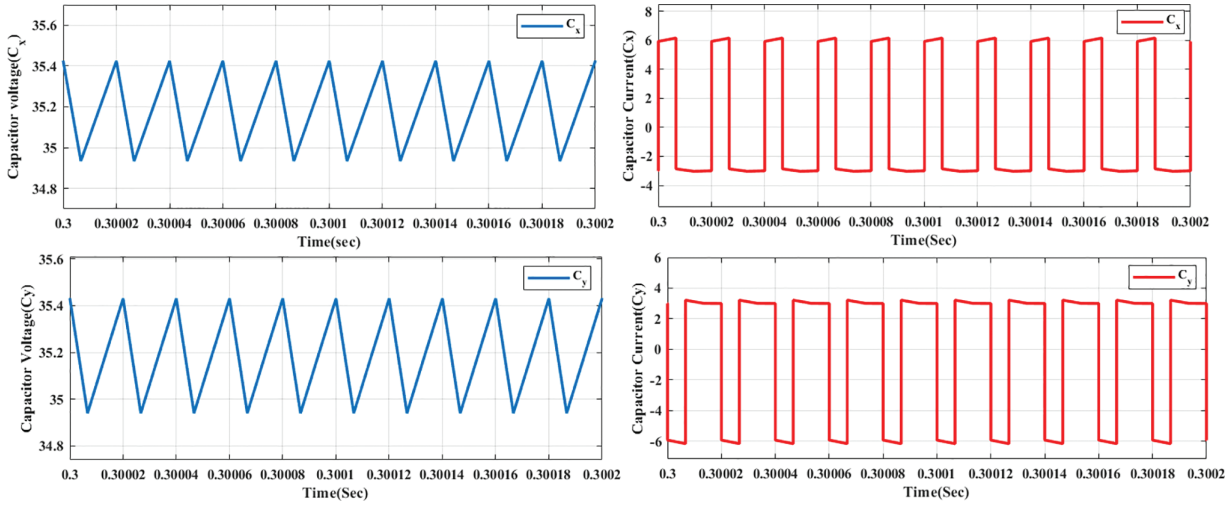


Figure 20: Capacitor voltage and current wave forms of C_x and C_y

The voltage and current waveforms of inductors L_x and L_y are given in Fig. 21. The inductor voltages should be positive and negative cycles while switching. These observations are evident of successful energy transfer. The inductor currents are operated in continuous conduction mode. The inductor L_x has an average current of 12 A with a ripple between 11.8−12.3 A while L_y carries an average bias current of approximately 6 A with a ripple between 5.8−6.2 A. All of these values correlate with expected theoretical values, thus validating the operation of the converter.

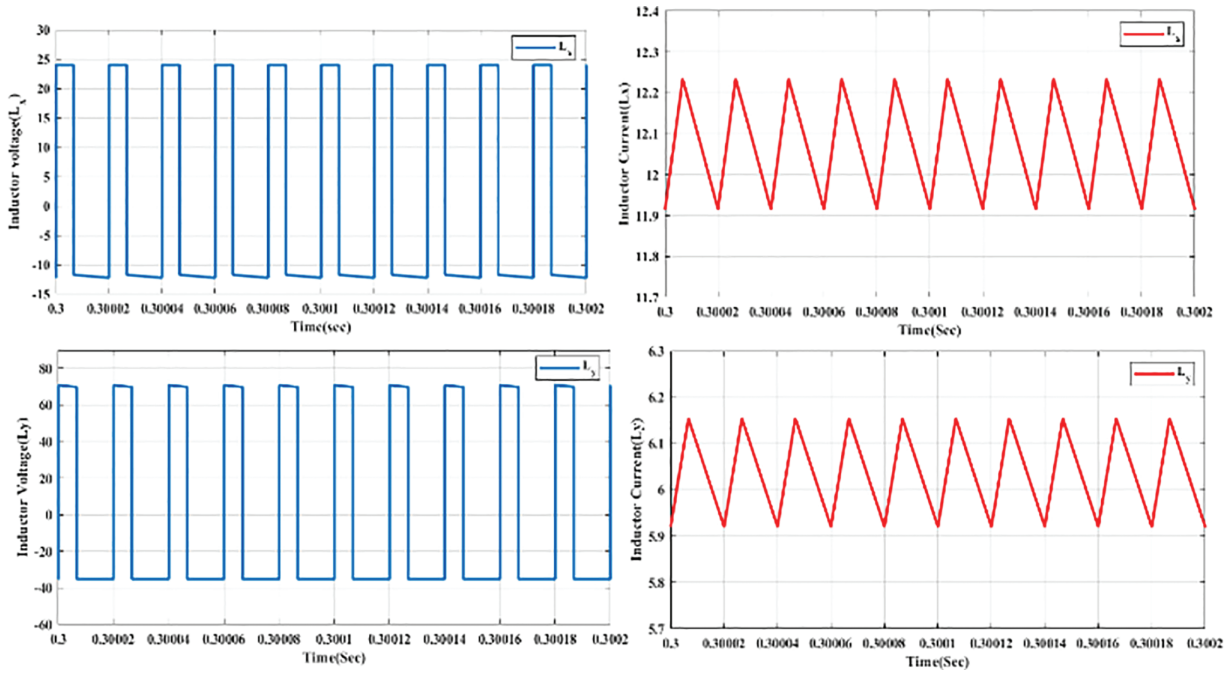


Figure 21: Inductor current and voltage wave forms of L_x and L_y

4.2 BLDC Motor Output Waveforms

The BLDC motor in Table 4 was coupled with the proposed DC–DC circuit and simulated to assess the performance of the complete drive. The converter provided a regulated output voltage of 72 V and at this output voltage, the BLDC motor pulls the rated current of 12.5 A and sustains rotor speed of 712 rpm, which is the operating speed. The torque constant of the motor is 0.85 Nm/A and the flux linkages is 0.4906 Wb, which allows for torque to be produced smoothly. Additionally, the low phase resistance of the motor 0.1 Ω and phase inductance of 0.5 mH allow for high dynamic response.

Table 4: BLDC motor specifications

Parameters	Specifications
Voltage	72 V
Current	12.5 A
Reference torque	3.5 Nm
Torque constant	0.85 Nm/A
Starting resistance	0.1 Ohms

(Continued)

Table 4 (continued)

Parameters	Specifications
Starting inductance	0.5 mH
Rotor speed	712 rpm
Magnetic Flux	0.4907 wb

The dynamic operation of the BLDC motor driving by the converter presented is shown by the speed and torque responses in Figs. 22 and 23. The speed waveform demonstrates a smooth raise from standstill to approximately 730 RPM without overshoot, assuming an operating condition of approximately 720 rpm based on the applied 72 V supply voltage. This indicates the achievable performance about voltage regulation and the stable interaction between the converter–motor.

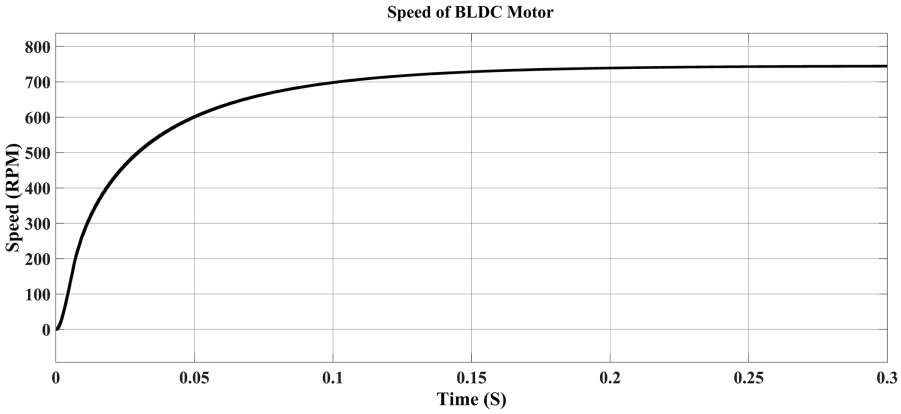


Figure 22: Rotor speed of the BLDC motor

The torque behaviour in Fig. 23 indicates proper operation as well. The reference torque is taken as constant of 3.5 Nm, and the motor torque is observed oscillating between 3–6 Nm acceptable. Overall, the results provide assurance that the motor is providing efficient and reliable performance with respect to the unique characteristics reported with the operation of the UGBC converter.

The back-EMF and phase current waveforms of the BLDC motor in Figs. 24 and 25 provide clear evidence of appropriate electrical commutation and uniform operation under the proposed converter drive. The back-EMF for phases A, B, and C all have an expected quasi-trapezoidal shape with peak values of around ±30–35 V, showing appropriate sinusoidal flux linkages and steady speed operation of the motor. The three waveforms are separated by 120°, confirming properly aligned rotor position with respect to the inverter switching sequence. Phase currents also follow the same six step commutation, oscillating around ±5–6 A depending on demand of torque. The currents are still synchronized with the zero-crossings of the back-EMF, helping to provide torque. The peaks of the higher frequency ripples in the currents are likely due to switching of the inverter characteristics. All the results indicate proper timing and excitation of the BLDC and further highlight the reliability of the drive.

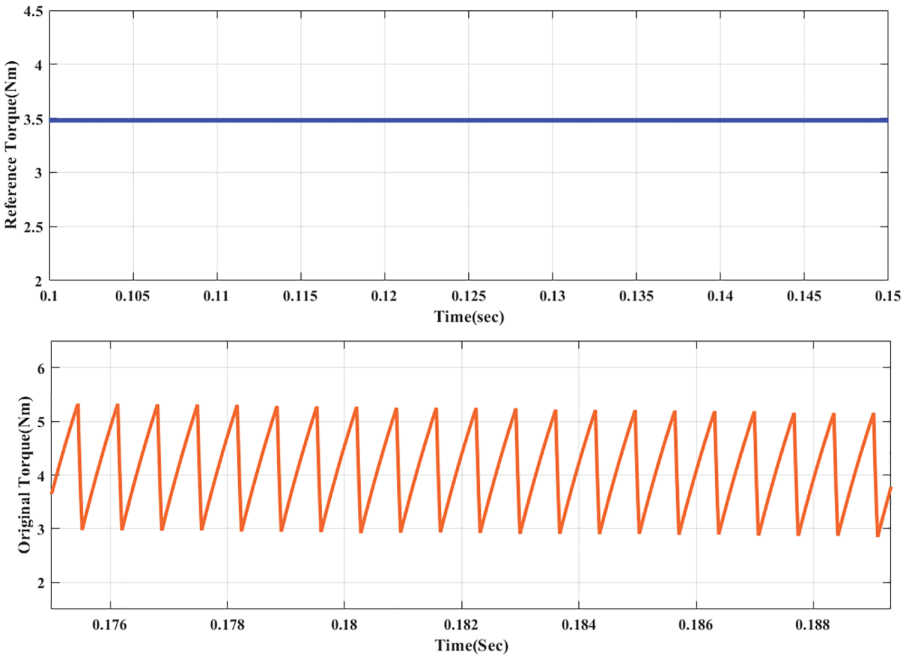


Figure 23: Simulated waveforms of reference and original torque

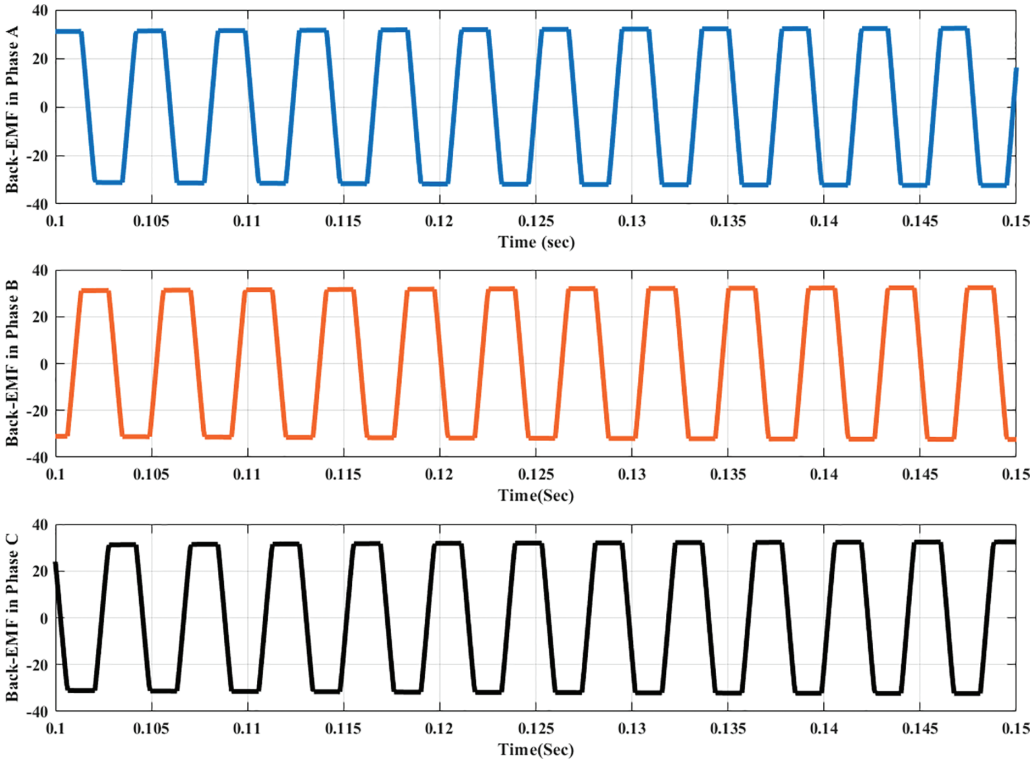


Figure 24: Back-EMF waveforms in phases A, B, and C of BLDC motor

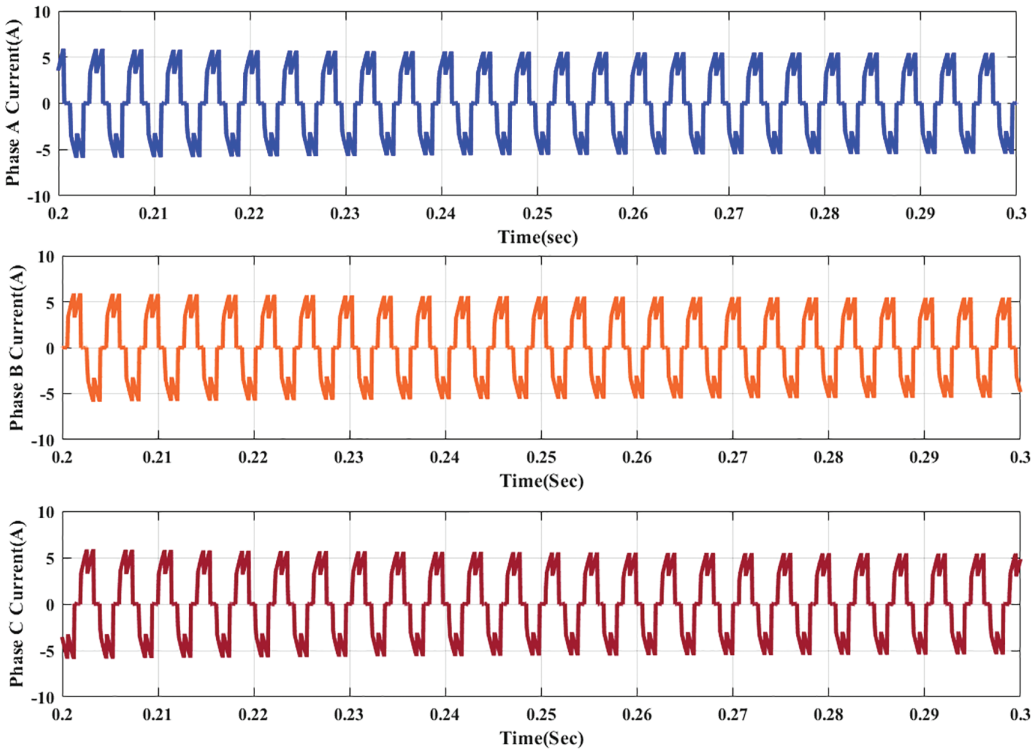


Figure 25: Phase currents of BLDC motor in phases A, B, and C

The output voltage response of the suggested high-gain DC–DC converter is given in Fig. 26. It shows that the output voltage quickly settles around 71 V as expected, in order to provide the required voltage-gain and drive the BLDC motor. A small transient overshoot can be seen, caused by the charging of the capacitors and building energy in the inductor. Certainly, this is common with high-gain topologies. After the transient period, the voltage continues to be highly stable, and has minimal ripple, indicating that the voltage is well regulated with a strong control. The steady output voltage of 72 V confirms that the converter operates efficiently, maintains the expected gain, and will provide a reliable DC link for motor-drive applications.

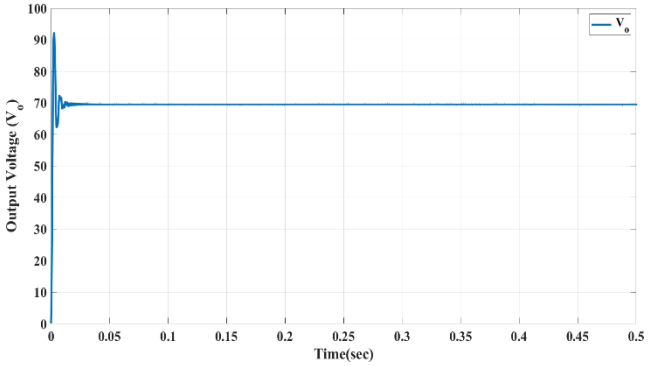


Figure 26: Output voltage waveform

The output current waveform of the intended converter is given in Fig. 27. The current follows the output voltage then reaching a stabilized value of approximately 4 A, corresponding to the expected load of the BLDC motor at a regulated output voltage of 72 V. There is a slight transient and overshoot for the first few milliseconds due to capacitor charging and establishing the steady-state inductor current and after that, the current is smooth and nearly ripple-free, indicating effective current regulation with continued conduction.

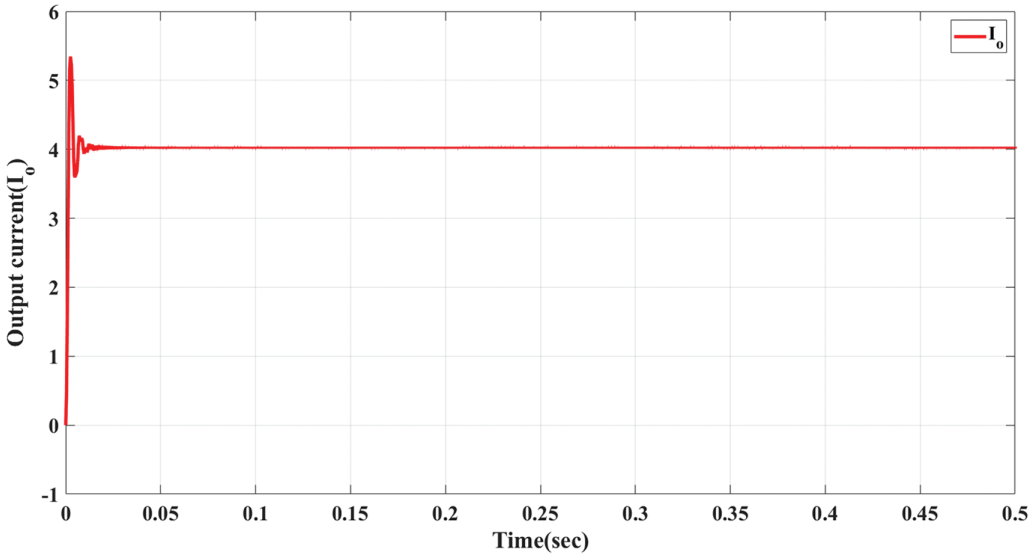
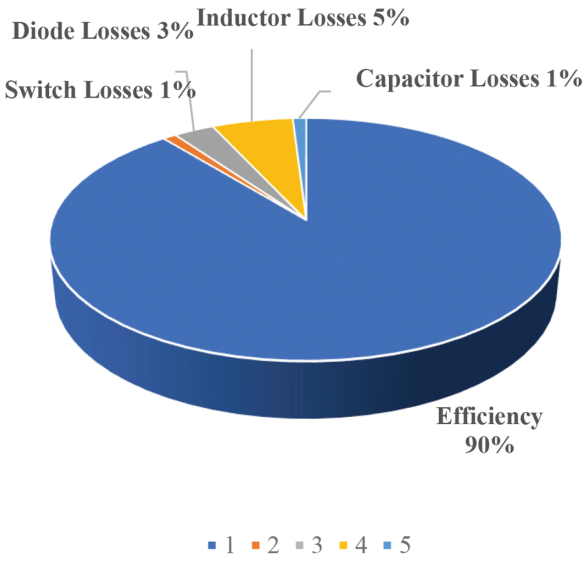
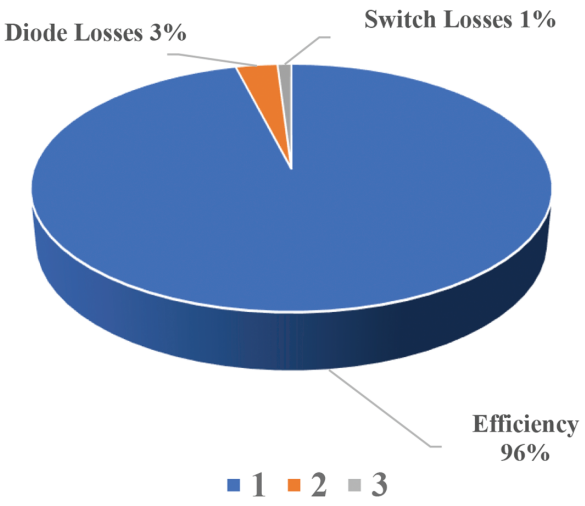


Figure 27: Output current waveform

The efficiency of the proposed UGBC configuration was tested under various power levels by changing the duty cycle, while keeping the load resistance fixed. The results of this test are shown in Fig. 28. At a duty ratio of 0.3, with the DC input of 24 V and a load resistance of 17.28 Ω, the configuration achieves an output voltage of 72 V. The results show that efficiency is lower at smaller duty ratios and gradually declines with further increases due to elevated load currents, which introduce higher conduction and switching losses. Fig. 28 provides a breakdown of the power losses across various circuit components using two pie charts. The first chart includes total losses, incorporating both passive (inductor and capacitor) and active component losses, while the second chart isolates active component losses by excluding those from passive elements, Fig. 28a. At the 0.3-duty ratio operating point, diode losses are the most significant contributors to overall power dissipation. Despite this, the converter demonstrates satisfactory efficiency, making it suitable for high-gain energy conversion applications Fig. 28b.



(a)



(b)

Figure 28: (**a**) Power losses including inductor and capacitor losses. (**b**) Power losses excluding inductor and capacitor losses

5 Conclusion

This paper presented the analysis and simulation-based validation of an Ultra Gain Boost Converter (UGBC) for solar-powered electric vehicle applications. The proposed UGBC is realized using a cascaded boost–boost configuration augmented with a capacitor–diode voltage-lift cell, which enables enhanced voltage gain at moderate duty ratios with continuous input current and reduced semiconductor stress. This structure avoids magnetic coupling and supports efficient operation with photovoltaic sources.

Comprehensive analytical modelling was carried out to evaluate the steady-state voltage gain, device stress, power losses, and small-signal dynamic behaviour of the converter. The analytical results were verified through MATLAB/Simulink simulations for an operating condition of 24 to 72 V at a duty ratio of 0.33. The results demonstrated stable output voltage regulation, low current ripple, and an efficiency exceeding 95%. A comparative analysis with recently reported high-gain DC–DC converters confirmed that the proposed UGBC offers a proper balance between voltage gain, device stress, and component count.

To examine system-level applicability, the UGBC was integrated with a brushless DC motor drive. The combined system shown stable speed regulation and smooth torque characteristics, indicating suitability for electric mobility applications. The present work is limited to analytical and simulation-based validation; experimental verification and closed-loop control implementation will be considered in future studies.

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Ethics Approval: Not applicable.

Conflicts of Interest: The authors declare no conflicts of interest.

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